

7th Generation Intel[®] Processor Families for U/Y Platforms and 8th Generation Intel[®] Processor Family for U Quad-Core and Y Dual Core Platforms

Datasheet, Volume 1 of 2

Supporting 7th Generation Intel[®] Core[™] Processor Families, Intel[®] Pentium[®] Processors, Intel[®] Celeron[®] Processors for U/Y Platforms and8th Generation Intel[®] Processor Family for U Quad Core formerly known as Kaby Lake Refresh and 8th Generation Intel[®] Processor Family inited undernood for Y Dual Core formerly known as Amber Lake 2-Core

ed undefined undefined undefined undefined undefined

Document Number: 334661-007

undermed underme undermed underme undefined undefi You may not use or facilitate the use of this document in connection with any infringement or other legal analysis concerning Intel products described herein. You agree to grant Intel a non-exclusive, royalty-free license to any patent claim thereafter drafted which includes subject matter disclosed herein.

No license (express or implied, by estoppel or otherwise) to any intellectual property rights is granted by this document.

Intel technologies' features and benefits depend on system configuration and may require enabled hardware, software or service activation. Performance varies depending on system configuration. No computer system can be absolutely secure. Check with your system manufacturer or retailer or learn more at intel.com.

Intel technologies may require enabled hardware, specific software, or services activation. Check with your system manufacturer or retailer.

The products described may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Intel disclaims all express and implied warranties, including without limitation, the implied warranties of merchantability, fitness for a particular purpose, and non-infringement, as well as any warranty arising from course of performance, course of dealing, or usage in trade.

All information provided here is subject to change without notice. Contact your Intel representative to obtain the latest Intel product specifications and roadmaps

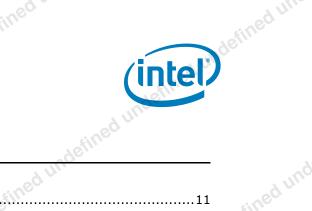
Copies of documents which have an order number and are referenced in this document may be obtained by calling 1-800-548-4725 or visit www.intel.com/design/literature.htm. No computer system can be absolutely secure.

.ation Intel, Core, Celeron, SpeedStep, Pentium, VTune, Xeon and the Intel logo are trademarks of Intel Corporation in the U.S. and/or other countries.

*Other names and brands may be claimed as the property of others.

All n All n undefined undefined undefined Copyright © 2020, Intel Corporation. All rights reserved.

ined undefined ! Datasheet, Volume 1 of 2 - A undefined



	defined undefine	ed undefined undefined .		ned
	nedu	Aunos	d	SLI,
	defill	stinec	(intel)	
d un		unde	10 Miles	
efines			dune	
Con	tents	*	stinet	
ed -	un ^o		uge.	
	AINEC	edv		
1 Intr				
1.1				
1.2		Managament		
		Management ment		
- d V	1.2.3 Memory Controller Pow	ver Management	14	
	1.2.4 Processor Graphics Pow	wer Management		
der	1.2.4.1 Memory Powe	er Savings Technologies		
duit	1.2.4.2 Display Powe 1.2.4.3 Graphics Core	r Savings Technologies e Power Savings Technologies		
1.3				
1.4	Package Support			
1.5				
1.6				9e,,
1.7 1.8				
	rfaces			
2.1		ology Supported		
der		Supported Memory Modules and I		
d un.	2.1.1.2 DDR4 Suppor	rted Memory Modules and Device	es	
		ported Memory Devices		
		g Support		
		ization Modes		
	2.1.5 Technology Enhanceme	ents of Intel [®] Fast Memory Acces	ss (Intel [®] FMA)26	9ein.
				Uc.
	2.1.7 DDR I/O Interleaving .			
2				
		n		
		ge Generation		
efined undefined 2.2				
ine ^o		pport		
Still	2.2.2 API Support (Windows	*)		
		QuickSync & Clear Video Techno		
		celerated Video Decode		Yeth
	2.2.3.3 Hardware Act	celerated Video Processing		
	2.2.3.4 Hardware Ace	celerated Transcoding		
Jefined undefine 2.3	2.2.5 Switchable/Hybrid Grap 2.2.6 Gen 9 LP Video Analyti	phics cs		
den		ion Low Power) Block Diagram		
- un		icy		
2.3	Display Interfaces	•		
let III.	2.3.1 DisplayPort*			
		edia Interface (HDMI*)		_
	2.3.3 Digital Video Interface2.3.4 embedded DisplayPort³	(DVI) * (eDP*)		196
	2.3.4 embeuded DisplayPort			INOS
	defin		0.0	
	un	(eDP*)		
Datasheet,	Volume 1 of 2	dur.	inde	
Datasheet,			du s	
unc		96, .	stine	
ed				
1etill.			du.	

	odefine	efineo		ned u
	Tred undefine	ndefined undefined s	od undefined unde	
(Intel		define	ofineo	
sine			under	
Inder		ions (Dual Channel DDR)		
	2.5.0 Multiple Display Configurat	ions (Single Channel DDR)	40	
	2.3.8 High-bandwidth Digital Cor	ntent Protection (HDCP)		
	2.3.9 Display Link Data Rate Sup 2.3.10 Display Bit Per Pixel (BPP)	pport Support		
	2.3.11 Display Resolution per Link	Width		
2.4	Platform Environmental Control Int			
3 Tech 3.1	nologies Intel [®] Virtualization Technology (Ir			
Jein 2.1	3.1.1 Intel [®] Virtualization Technol	ology (Intel [®] VT) for IA-32, In	ntel [®] 64 and Intel [®]	
d une	Architecture (Intel [®] VT-X).			
3.2	3.1.2 Intel [®] Virtualization Technologies	ology (Intel $^{ extsf{R}}$ VT) for Directed	1/0 (Intel [©] VI-d) 49	
	3.2.1 Intel [®] Trusted Execution To	echnology (Intel [®] TXT)		
	3.2.2 Intel [®] Advanced Encryption 3.2.3 PCLMULODO (Perform Carr	n Standard New Instructions (y-Less Multiplication Quad wo	Intel [®] AES-NI) 53	
	3.2.4 Intel [®] Secure Key			
	3.2.5 Execute Disable Bit			
y ur		ecution Protection (SMEP)		
	3.2.8 Intel [®] Supervisor Mode Ac	cess Protection (SMAP)		
der		Extensions (Intel [®] MPX)		
dui	3.2.10 Intel [®] Software Guard External 3.2.11 Intel [®] Virtualization Technol	ensions (Intel® SGX) aloay (Intel® VT) for Directed		
3.3	Power and Performance Technologi	ies		
		chnology (Intel [®] HT Technolog		
		logy 2.0 st Technology 2.0 Frequency		retine
	3.3.3 Intel [®] Advanced Vector Ex	tensions 2 (Intel [®] AVX2)		
	3.3.4 Intel [®] 64 Architecture x2A 3.3.5 Power Aware Interrupt Rou			
Jeffmed undefin3.4	3.3.6 Intel [®] Transactional Synch	ronization Extensions (Intel [®]	TSX-NI)59	
3.4	Intel [®] Transactional Synchronization	on Extensions (Intel [®] TSX-NI)	provides a set of	
inde	instruction set extensions that allow transactional synchronization. Prog			
ed u	performance of fine-grain locking v	vhile actually programming us	ing coarse-grain locks.	
efill	Details on Intel TSX-NI may be fou Programming Reference.Intel TSX-	NI may not be available on all	LSKUs Intel® Image	
	Signal Processor (Intel [®] ISP) 3.4.1 Intel [®] Image Signal Proces	(,) ()		0
3.5	3.4.1 Intel [®] Image Signal Proces The Intel ISP is an embedded came	sor (Intel [®] ISP) ra subsystem bardware comp	onent on the processor	gein
5.5	it processes video and still images	at high quality with a low-pow	/er cost by leveraging a \searrow	
	programmable VLIW (very-long-ins) fixed function pipe (accelerators), t			
ned	accelerators and compute capabilit	ies allows the flexibility and pa	atchability that are	
defin	required for late changes and allowi remaining in an optimized power p	ng the unit to support future se erformance point.Debug Tech	ensor technologies while nologies	
d une	3.5.1 Intel [®] Processor Trace			
A Pow	er Management			
4.1	Advanced Configuration and Power	Interface (ACPI) States Supp	orted 64	
defined undefine 4.1 4.2	Processor IA Core Power Managem 4.2.1 OS/HW controlled P-states			, Sil
	4.2.1.1 Enhanced Intel [®]	SpeedStep [®] Technology		Inde.
4 aetined undefined	den	efine		
4	UI.	unde	Datasheet, Volume 1 of 2	
- stine			Butasheet, volume 1 01 2	
inde	Aefil		siner	
	- une		nder	
1efill		6-	U.	



ndefined undefined unf		undefine undefined undefi		ed un
		under		define
	stine	redu	(intel	P
un		defil	(inter	
ined t		d une	inde	
defin		4.2.1.2 Intel [®] Speed Shift Technology	67	,
dun	4.2.2	Low-Power Idle States	67	7
	4.2.3	Requesting Low-Power Idle States		
der	4.2.4 4 2 5	Processor IA Core C-State Rules Package C-States		dull
	4.2.5	Package C-States and Display Resolutions		sineu
4.3		ted Memory Controller (IMC) Power Managemen	nt74	r ger
	4.3.1	Disabling Unused System Memory Outputs		
71.	4.3.2	DRAM Power Management and Initialization 4.3.2.1 Initialization Role of CKE		r
		4.3.2.2 Conditional Self-Refresh))
Alle		4.3.2.3 Dynamic Power-Down		5
inde	4 2 2	4.3.2.4 DRAM I/O Power Management		
	4.3.3 4.3.4	DDR Electrical Power Gating (EPG) Power Training		
4.4		for Graphics Power Management		, inc
Inde	4.4.1	Memory Power Savings Technologies		
		4.4.1.1 Intel [®] Rapid Memory Power Manager 4.4.1.2 Intel [®] Smart 2D Display Technology	nent (Intel [®] RMPM)77	stine
	4.4.2	Display Power Savings Technologies		
	yetti,	4.4.2.1 Intel [®] (Seamless & Static) Display Re	efresh Rate	
<u>,</u> 0	nc.	Switching (DRRS) with eDP* Port		}
		4.4.2.2 Intel [®] Automatic Display Brightness . 4.4.2.3 Smooth Brightness		; }
defin		4.4.2.4 Intel [®] Display Power Saving Technolo	ogy (Intel [®] DPST) 6.078	}
, unc.		4.4.2.5 Panel Self-Refresh 2 (PSR 2) 4.4.2.6 Low-Power Single Pipe (LPSP))
	4.4.3	4.4.2.6 Low-Power Single Pipe (LPSP) Processor Graphics Core Power Savings Technol		
defin	1.1.5	4.4.3.1 Intel [®] Graphics Dynamic Frequency		
une		4.4.3.2 Intel [®] Graphics Render Standby Tech	nnology (Intel [®] GRST)80	
4.5	System	4.4.3.3 Dynamic FPS (DFPS) Agent Enhanced Intel [®] Speedstep [®] Technolog		defini
4.5	Voltag	Optimization		L UNC.
5 Theri	76-	nagement		
		or Thermal Management		
5.10 Jundefined undefine	5.1.1	Thermal Considerations		
	5.1.2	Intel [®] Turbo Boost Technology 2.0 Power Moni		
ed u.	5.1.3	Intel [®] Turbo Boost Technology 2.0 Power Cont 5.1.3.1 Package Power Control		
afine		5.1.3.2 Platform Power Control		3
		5.1.3.3 Turbo Time Parameter (Tau)		
	5.1.4	Configurable TDP (cTDP) and Low-Power Mode 5.1.4.1 Configurable TDP		
		5.1.4.2 Low-Power Mode		
	5.1.5	Thermal Management Features		
	unc	5.1.5.1 Adaptive Thermal Monitor 5.1.5.2 Digital Thermal Sensor		7
in ^{e0}		5.1.5.3 PROCHOT# Signal		
defin		5.1.5.4 Bi-Directional PROCHOT#)
A UNC		5.1.5.5 Voltage Regulator Protection using PR 5.1.5.6 Thermal Solution Design and PROCHO		
		5.1.5.7 Low-Power States and PROCHOT# Be		
delli		5.1.5.8 THERMTRIP# Signal		
a une		5.1.5.9 Critical Temperature Detection 5.1.5.10 On-Demand Mode		sineu
ed undefined undefined		5.1.5.11 MSR Based On-Demand Mode		den
		5.1.5.11 MSR Based On-Demand Mode	ehavior	dun
	Inde	Aeth.		le
Datasheet, V	olume 1 o	2 4 11/12	nder	-
Datasheet, V			ad un	5
, uno-		den	stine	
		dull	inde	
10fm			du	

		adefine	efil		aned un
(in	tel	ined undefine	d undefined undefin	eine	ed undefined un
ed undefine	5.2	5.1.5.12 I/O Emulatio 5.1.6 Intel [®] Memory Therma	al Management r (SDP)	Jue	91 91 91
	-	5.2.1 KBL U/Y Processor Line	e Thermal and Power Sp	ecifications	93
6	6.1 6.2 6.3 6.4 6.5 6.6 6.7	I Description System Memory Interface Reset and Miscellaneous Signa embedded DisplayPort* (eDP* Display Interface Signals Testability Signals Error and Thermal Protection S Power Sequencing Signals	ils) Signals Signals		95 99 100 100 100 101 102
neu	6.8 6.9	Processor Power Rails Ground, Reserved and Non-Cri	itical to Function (NCTF)	Signals	104
7	6.10	Processor Internal Pull-Up / Pu rical Specifications			104
	7.1 7.2	$\begin{array}{llllllllllllllllllllllllllllllllllll$	s ion (VID)		105 105 105
ined undefin		7.2.1.1 Vcc DC Species 7.2.1.2 Vcc _{GT} and Vc 7.2.1.3 VDDQ DC Sp 7.2.1.4 VccSA DC Sp 7.2.1.5 VccIO DC Sp 7.2.1.6 VccOPC DC Sp 7.2.1.7 VccEOPIO DC 7.2.1.8 Vcc _{OPC_1p8}	ifications cc _{GTX} DC Specifications pecifications ecifications specifications C Specifications C Specifications becifications		106 108 110 110 112 112 113 113 114
stined undefin	led ut	7.2.1.10 VCCPLL DC S 7.2.2 Processor Interfaces D 7.2.2.1 DDR3L/-RS I 7.2.2.2 LPDDR3 DC S 7.2.2.3 DDR4 DC Sp 7.2.2.4 Digital Displa 7.2.2.5 embedded D 7.2.2.6 CMOS DC Sp 7.2.2.7 GTL and OD 7.2.2.8 PECI DC Cha	C Specifications DC Specifications Specifications ecifications ay Interface (DDI) DC Sp isplayPort* (eDP*) DC Sp ecifications DC Specifications	pecifications pecification	116 116 117 118 119 119 119 119 120
8	Packa	age Mechanical Specification			124
	8.1 8.2	Package Mechanical Attributes Package Loading Specifications	s		124
9 undefi	0 1	Package Storage Specifications Quad Core/YProcessor BallI U-Processor and U-Quad Core Y-Processor Ball Information	nformation		126 126
efined undefi		Y-Processor Ball Information	Processor Ball Informati	defined under	etined undefine
		define	afineo		ned un
6	ined	-9 ///	efined unde	Datasheet, Volume	1 of 2
lefined -		med une		od unde.	



9e1.		undefined undefine		atimed undefined s		defined un
		nde		AGUI.		
		du.		inos		9em
		der		Stine	(Intel	
					1 efthe	
	- neo		d Un.			
	1 clill				du	
	Figure	es	ACTIN			
90	1-1		I AML-Y22 Processor L	ine Platforms		
	2-1	Intel [®] Flex Memory Te	echnology Operations			
Jer.	2-2	Interleave (IL) and No	on-Interleave (NIL) Mo	odes Mapping	27	
	2-3	Video Analytics Comm	on Use Cases			09
	2-4	Gen 9 LP Block Diagra	ım			(All)
	2-5			ports as an example)		
	2-6	DisplayPort* Overview	v			
	2-7					
	2-8			<u>></u>		
	2-9					
	3-1					
	3-2					
	3-3	Platform Imaging Infra	astructure			
	4-1					
	4-2					
	4-3			Processor IA Cores		
	4-4					
	5-1					
	7-1					
	9-1			_eft, Columns 71-48)		
				Middle, Columns 47-24).		
				Right, Columns 23-1)		
	9-4			_eft, Columns 71-48)		
	9-5			Middle, Columns 47-24).		
	9-6			Right, Columns 23-1)		
in the second se	9-7			64-44)		
	9-8			ns 43-23)		
UI.	9-9			s 42-1)		
				64-44)		
				ns 43-23)		
	9-12	Y-Processor Ball Map ((Lower Right, Column	s 42-1)		
		UN		nden	Sino	
	Table	_ 0 ~	ر س	(n-	de	
		-	eo		2 UL	
	1-1	Processor Lines	ofille		11	
	1 2					

	F-Processor Bail Map (Opper Right, Columns 42-1)	
	9-10 Y-Processor Ball Map (Lower Left, Columns 64-44)	Yelli
9-	0-11 Y-Processor Ball Map (Lower Middle, Columns 43-23)	
9-	9-12 Y-Processor Ball Map (Lower Right, Columns 42-1)	
	bles -1 Processor Lines	
Tab	bles ^d d ^{unc} n ^{der}	
Iau		
96		
- · · · -	-1 Processor Lines	
	-2 Terminology	
	-3 Related Documents	
	2-1 Processor DRAM Support Matrix	-90
2-	2-2 Supported DDR3L/-RS Non-ECC SO-DIMM Module Configurations	
2	(U-Processor Line)	Yell
Ζ-	2-3 Supported DDR3L/-RS Memory Down Module Configurations (U-Processor Line)	
٦.	A Supported DDD/ Nep ECC SCDIMM Medule Contigurations	
2	(U/U-4 Core Processor Line)	
2.	2-5 Supported DDR4 Memory Down Device Configurations	
2	2-5 Supported DDR4 Memory Down Device Configurations (U/U-4 Core Processor Line)	
2.	2-6 Supported LPDDR3 x32 DRAMs Configurations	
	 Supported LPDDR3 x32 DRAMs Configurations (KBL Y/H/U/U-4 Core and AML-Y22 Processor Lines)	
2-	2-7 Supported LPDDR3 x64 DRAMs Configurations	
efil .	(KBL Y/U/U-4 Core and AML-Y22 Processor Lines)	
2-	2-8 DRAM System Memory Timing Support	
2.	2-9 DRAM System Memory Timing Support (LPDDR3)24	
2.	2-10 Interleave (IL) and Non-Interleave (NIL) Modes Pin Mapping	der.
	eine	700
	der	
	une ade.	
Data	tasheet, Volume 1 of 2	
	ineu d'un l	
	tasheet, Volume 1 of 2 defined undefined undef	
dui	ino-	
	du	
76/1.		

961.		define		ned	ed une
		hed undefine	ad undefined undefi		d undefined une
(i	nte				dune
Ċ			inder	define	
efin			² d ¹	d unc.	
4 UNOC		Hardware Accelerated Video Deco Hardware Accelerated Video Enco	/uning		29
	2-13	Switchable/Hybrid Graphics Supp	ort		32
nder.		GT2/3 Graphics Frequency (KBL UVGA and Embedded DisplayPort*			
	2-16	Embedded DisplayPort (eDP*)/DD	DI Ports Availability	<u></u>	34
		Display Technologies Support Display Resolutions and Link Band			
	2-19	Processor Supported Audio Forma	ats over HDMI and Displ	layPort [*]	40
		Maximum Display Resolution Y/AML Y22-Processor Lines Displ			
1 and 1		U/U-4 Core Processor Lines Displ			
unde		U/U- 4 Core Processor Lines Disp			
ined t		HDCP Display supported Implication Display Link Data Rate Support			
defin	2-26	Display Resolution and Link Rate	Support		43
		Display Bit Per Pixel (BPP) Supported Resolutions1 for HBR			
		Supported Resolutions1 for HBR2	2 (5.4 Gbps) by Link Wi	dth	44
	4-1 4-2	System States Processor IA Core / Package State	e Support		64
		Integrated Memory Controller (IM	IC) States		65
	4-4 4-5	PCI Express* Link States Direct Media Interface (DMI) Stat			
nde	4-5	G, S, and C Interface State Comb			
ed u.	4-7	Deepest Package C-State Availab			
define	4-8 5-1	Targeted Memory State Condition Configurable TDP Modes			
uno	5-2	TDP Specifications (KBL U/Y/AML-	-Y22 Processor Line)		93
	5-3 5-4	Package Turbo Specifications (KB Junction Temperature Specification			
	6-1	Signal Tables Terminology			95
	6-2 6-3	DDR3L/-RS Memory Interface LPDDR3 Memory Interface			
	6-4	DDR4 Memory Interface	<u></u>		97
	6-5 6-6	System Memory Reference and C Reset and Miscellaneous Signals.	ompensation Signals		99 99
d un.	6-7	embedded DisplayPort* Signals			100
lefine	6-8 6-9	Display Interface Signals Testability Signals			
undefined unde		Error and Thermal Protection Sign			
	6-11	Power Sequencing Signals		<u> </u>	102
		Processor Power Rails Signals GND, RSVD, and NCTF Signals			
	6-14	Processor Internal Pull-Up / Pull-E	Down Terminations		104
	7-1 7-2	Processor Power Rails Processor IA core (Vcc) Active and			
	7-3	Processor Graphics (Vcc _{GT} and Vcc	C _{GTX}) Supply DC Voltage	e and Current Specifications	108
dun	7-4 7-5	Memory Controller (VDDQ) Suppl System Agent (VccSA) Supply DC			
	7-6	Processor I/O (VccIO) Supply DC	Voltage and Current Sp	ecifications	112
inde.	7-7 7-8	VCC _{OPC} Voltage levels Processor OPC (Vcc _{OPC}) Supply D			
d undefined un	7-9	VCC _{EOPIO} Voltage levels (separate	e VR)	<u>~</u> ~~	113
	7-10	Processor EOPIO (Vcc _{EOPIO}) Supp	ly DC Voltage and Curre	ent Specifications	113
s actined un		4 unde	etined under the		efined u.
8			ed un.	Datasheet, Volume :	1 of 2
	9611		efine	od undefined un	
ed u		unc		aden.	
etine				dui	



	define			ed un
7-11 Proce 7-12 Vcc S 7-13 Vcc S 7-14 Proce 7-15 Proce 7-16 DDR3	od unc	undefined undefined s	(intel)	define
	Inec		(intol)	
d unos		nden	line	
efinec	ined			
7-11 Proce 7-12 Vcc S	ssor OPC (Vcc _{OPC_1p8}) Supply DC ustain (VccST) Supply DC Voltage		cations113	
7-13 Vcc S	ustain Gated (VccSTG) Supply DC	C Voltage and Current Specif	ications114	
7-14 Proce 7-15 Proce	ssor PLL (VccPLL) Supply DC Volt ssor PLL_OC (VccPLL_OC) Supply	DC Voltage and Current Spe	ecifications115	ed l
	L/-RS Signal Group DC Specificat R3 Signal Group DC Specification			define
7-18 DDR4	Signal Group DC Specifications . I Display Interface Group DC Spe			
7-20 embe	dded DisplayPort* (eDP*) Group	DC Specifications		
	Signal Group DC Specifications. ignal Group and Open Drain Sigr			
7-23 PECI 8-1 Packa	DC Electrical Limits ge Mechanical Attributes			
8-2 Packa	ge Loading Specifications			
9-1 U/U-C	Quad Core Processor Ball List			ed
9-2 Y-Pro	cessor Ball List	unde:		defill
2	efine		ed	
d une		inder	define	
lefines			d une	
d unoc	nden		define	
atinec	ined U.		uno	
	defill	lefine.		
	ed un.	4 UNOP		ndefin
	Jefine	stineo	equilibrium of the second seco	Ult
dun		under	define	
			ed une	
d unc	Inder		define	
efinee	inedu		UNC	
	nden	define.		
	nedu	d unou		ndein
	defili	efinet	e	30.
ed ul		y unde	adefin	
define			ed un	
d un	inder		define	
afine			dun	
	ndefine	terine		
	ignal Group and Open Drain Sigr DC Electrical Limits ge Mechanical Attributes ge Loading Specifications ge Storage Specifications Juad Core Processor Ball List cessor Ball List	d undefine		indefin

	undefine	adefined		
(inte		undefined un	defin	ed unde
Rev	ision His	tory	Indefined un	
	ndefine	Letined		
Revision Number	sined un	Description	Revision I	Date
001	 Initial release 	18AND	August 20	016
defined	 Intel[®] Celeron[®] proce Intel[®] Pentium[®] proc 	lowing processors ⁰ Core™ processors i7-7600U, i5-7300U, i7-7Y75, i5 7560U, i5-7360U, i5-7287U, i5-7267U, i5-7260U, i3- essors 3965U, 3865U ressors 4415U, 4410Y	-7Y57, i7- 7167Ú	
002	 Updated table 2-24, "HDC HDMI2.0 changed from 4 Updated Section 5.1, "Pro Updated Section 5.1.1-"T Updated Section 5.1.5.1. 	ocessor Thermal Management". hermal Considerations".	ions for January 2	017
ndefined	 Updated table 5-3, "Packa Updated Table 7-2, "Proce Specifications". Updated Table 7-3, "Proce Specifications". 	age Turbo Specifications (U/Y-Processor Line) . age Turbo Specifications (U/Y-Processor Line)" + Add essor IA core (Vcc) Active and Idle Mode DC Voltag essor Graphics (VccGT and VccGTX) Supply DC Voltag em Agent (VccSA) Supply DC Voltage and Current Sp	and Current e and Current	inec
003	 Updated Table 2-18, "Disp Calculations". Updated TOB parameter i Updated Table 7-2, "Proce Specifications", Note 14. Updated Table 7-3, "Proce Specifications", Note 10. 	neration Intel [®] Processor Family for U Quad Core Pla play Resolutions and Link Bandwidth for Multi-Stream n Chapter 7. essor IA core (Vcc) Active and Idle Mode DC Voltage essor Graphics (VccGT and VccGTX) Supply DC Voltag em Agent (VccSA) Supply DC Voltage and Current Sp	and Current August 20	oir Sined un
004	Added Section 1.6, Operation	ating System Support	September	2018
005	Updated document title	76UL.	December 2	2018
006	Updated Section 1.6, Ope	erating System Support	January 2	019
005 006 007	Updated Section 7.1.2 VC		August 20	fined
undefine	Updated Section 7.1.2 VC	Erating System Support	ned undefined und	61.
10	ed undefined w.	defined undefined unoc	Datasheet, Volume	a 1 of 2
		ed un	y unde.	

Introduction



Introduction

Processor Volatility statement:

Intel[®] Kaby Lake processor families does not retain any end user data when powered down and/or when the processor is physically removed.

Note:

Power down refers to state which all processor power rails are off.

The 7th Generation Intel[®] Core[™] processor, Intel[®] Pentium[®] processor, Intel[®] Celeron[®] processor families and 8th Generation Intel[®] Processor Family for U 4-Core and Y-2 Core family are 64-bit, multi-core processors built on 14-nanometer process technology.

The U-Processor Line and Y-Processor Line are offered in a 1-Chip Platform that includes the 7th Generation Intel[®] processor families I/O Platform Controller Hub (PCH) die on the same package as the processor die. See the following figure.

Some of the processor SKUs are offered with On-Package Cache.

The following table describes the processor lines covered in this document.

Processor Line ¹	Package	Base TDP	Processor IA Cores	Graphics Configuration	On-Package Cache	Platform Type
KBL Y-Processor Line	BGA1515	4.5W	2	GT2	N/A	1-Chip
KBL Y-Processor Line With Integrated HDCP2.2	BGA1515	4.5W	2	GT2	N/A	1-Chip
KBL Y-Pentium/Celeron Processor Line	BGA1515	6W	062	GT2	N/A	1-Chip
AML-Y Processor Line (2- Cores)	BGA1515	5W cd	2	GT2	N/A	1-Chip
KBL U-Processor Line	BGA1356	15W	2	GT2	N/A	1-Chip
KBL U-Processor Line	BGA1356	15W	2	GT2	N/A	1-Chip
With Integrated HDCP2.2	BGA1356	15W, 28W	2	GT3	64 MB	1-Chip
KBL U-Pentium/Celeron Processor Line	BGA1356	15W	2	GT1	N/A	1-Chip
KBL U-Processor Line (U- 4 Core)	BGA1356	15W	4	GT2	N/A	1-Chip

Table 1-1. **Processor Lines**

Throughout this document, the 7th Generation Intel[®] Core[™] processor, Intel[®] Pentium[®] processor, Intel[®] Celeron[®] processor, and 8th Generation Intel[®] Processor Family for U 4-Core family (known as KBL-U Refresh) and Y 2-Core (named Amber Lake)may be referred to simply as "processor". The 7th Generation Intel[®] processor A undefined undefined undefined families I/O and 8th Generation Intel[®] Processor Family for U 4-Core and Y 2-Core family I/O Platform Controller Hub (PCH) may be referred to simply as "PCH".

This document is for the following U/Y-Processor SKUs:

Datasheet, Volume 1 of 2

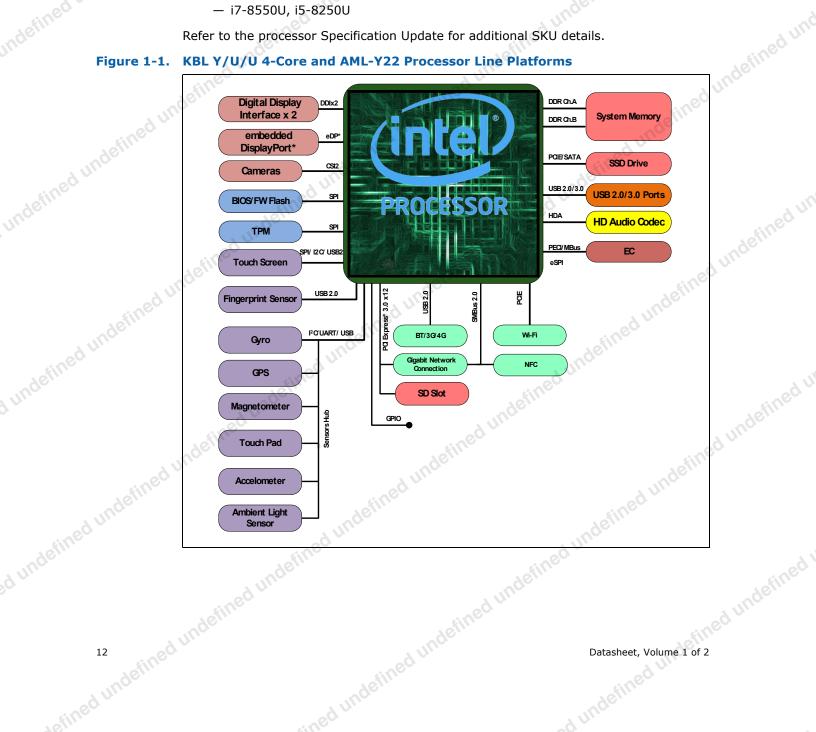


intel red under

- ed undefined undefined 7th Generation Intel[®] Core[™] processor family U-Processors
 - ed undefined undefined unde i7-7500U, i5-7200U, i3-7100U, i7-7600U, i5-7300U, i7-7660U, i7-7567U, i7-7560U, i5-7360U, i5-7287U, i5-7267U, i5-7260U, i3-7167U
- 7th Generation Intel[®] Core[™] processor family Y-Processors
 - i7-7Y75, i5-7Y54, m3-7Y30, i7-7Y75 with vPro[™] support, i5-7Y57
- Intel[®] Pentium[®] processors
 - 4415U, 4410Y
- Intel[®] Celeron[®] processors
 - 3965U, 3865U
- 8th Generation Intel[®] Processor Family for U Quad Core family
 - i7-8550U, i5-8250U

Refer to the processor Specification Update for additional SKU details.

Figure 1-1. KBL Y/U/U 4-Core and AML-Y22 Processor Line Platforms



Datasheet, Volume 1 of 2 -4 undefined



Introduction

Supported Technologies

- Intel[®] Virtualization Technology (Intel[®] VT)
- Intel[®] Active Management Technology 11.0 (Intel[®] AMT 11.0)
- Intel[®] Trusted Execution Technology (Intel[®] TXT)
- Intel[®] Streaming SIMD Extensions 4.2 (Intel[®] SSE4.2)
- Intel[®] Hyper-Threading Technology (Intel[®] HT Technology)
- Intel[®] 64 Architecture
- Execute Disable Bit
- Intel[®] Turbo Boost Technology 2.0
- Intel[®] Advanced Vector Extensions 2 (Intel[®] AVX2)
- Intel[®] Advanced Encryption Standard New Instructions (Intel[®] AES-NI)
- PCLMULQDQ (Perform Carry-Less Multiplication Quad word) Instruction
- Intel[®] Secure Key
- Intel[®] Transactional Synchronization Extensions (Intel[®] TSX-NI)
- PAIR Power Aware Interrupt Routing
- SMEP Supervisor Mode Execution Protection
- Intel[®] Boot Guard
- On-package Cache Memory
- Intel[®] Software Guard Extensions (Intel[®] SGX)
- Intel[®] Memory Protection Extensions (Intel[®] MPX)
- GMM Scoring Accelerator
- Intel[®] Image Signal Processor (Intel[®] ISP)
- Intel[®] Processor Trace
- High-bandwidth Digital Content Protection (HDCP)

The availability of the features may vary between processor SKUs

Refer to Chapter 3, "Technologies" for more information.

Power Management Support 1.2

1.2.1 Processor Core Power Management

- Full support of ACPI C-states as implemented by the following processor C-states: - C0, C1, C1E, C3, C6, C7, C8, C9, C10
- Enhanced Intel SpeedStep[®] Technology

Refer to Section 4.2, "Processor IA Core Power Management" for more information. A undefined undefined undefined

Note:





1.2.2 System Power Management

• S0/S0ix, S3, S4, S5

Refer to Chapter 4, "Power Management" for more information.

1.2.3 Memory Controller Power Management

- Disabling Unused System Memory Outputs
- DRAM Power Management and Initialization
- Initialization Role of CKE
- Conditional Self-Refresh
- Dynamic Power Down

Refer to Section 4.3, "Integrated Memory Controller (IMC) Power Management" for more information.

1.2.4

1.2.4.1 **Memory Power Savings Technologies**

- Intel Rapid Memory Power Management (Intel RMPM)
- Intel Smart 2D Display Technology (Intel S2DDT)

Display Power Savings Technologies 1.2.4.2

- Intel (Seamless & Static) Display Refresh Rate Switching (DRRS) with eDP port
- Intel Automatic Display Brightness
- Smooth Brightness
- Intel Display Power Saving Technology (Intel DPST 6)
- Panel Self-Refresh 2 (PSR 2)
- Low Power Single Pipe (LPSP)

1.2.4.3 **Graphics Core Power Savings Technologies**

- Intel Graphics Dynamic Frequency
- Intel Graphics Render Standby Technology (Intel GRST)
- Dynamic FPS (Intel DFPS)

Refer to Section 4.4, "Processor Graphics Power Management" for more information. warned undefined undefined undefined in a undefined undefined undefined

Datasheet, Volume 1 of 2 A undefined

(intel) defined ut

Introduction

defined undefined 1

Thermal Management Support

- Digital Thermal Sensor
- Intel Adaptive Thermal Monitor
- THERMTRIP# and PROCHOT# support
- On-Demand Mode
- Memory Open and Closed Loop Throttling
- Memory Thermal Throttling
- External Thermal Sensor (TS-on-DIMM and TS-on-Board)
- Render Thermal Throttling
- Fan speed control with DTS
- Intel Turbo Boost Technology 2.0 Power Control

Refer to Chapter 5, "Thermal Management" for more information.

Package Support

The processor is available in the following packages:

- A 20.5 mm x 16.5 mm BGA package (BGA1515) for Y/ AML- Y22 Processor Line
- A 42 mm x 24 mm BGA package (BGA1356) for U/U-4 Core Processor Line

1.5 Processor Testability

An XDP on-board connector is warmly recommended to enable full debug capabilities. For the processor SKUs, a merged XDP connector is highly recommended to enable lower C-state debug.

Note:

01.4

When separate XDP connectors will be used at C8–C10 states, the processor will need to be waked up using the PCH.

Datasheet, Volume 1 of 2

ad undefined undefined The processor includes boundary-scan for board and system level testability.

Operating Systems Support

	4 UNOC	(7	th Gen)			lefinec
	Processor Line	Windows* 10 64-bit	ne ^d os x	Linux* OS	Chrome* OS	Inde
nu .	U-processor line	Yes	Yes	Yes	Yes	
	Y-processor line	Yes	Yes	Yes	Yes	
1efill.		and et			200	1
unos	Ś	ein. (8	th Gen)	Sint		
	Processor Line	Windows* 10 64-bit	OS X	Linux* OS	Chrome* OS	
	U-processor line	Yes	Yes	Yes	Yes	6
	Y-processor line	Yes	Yes	Yes	Yes	stine
1.7	Terminology		ed un		2	unos

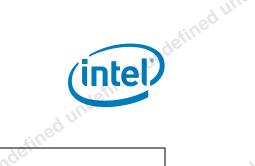
1.7 Terminology

(intel) and under

Table 1-2. undefined undefi

Terminology (Sheet 1 of 3)

undefined undefin	Term	Description	
dull	4К	Ultra High Definition (UHD)	
sinec	AES	Advanced Encryption Standard	
nder	AGC	Adaptive Gain Control	undefined un
U	BLT	Block Level Transfer	sines
	BPP	Bits per pixel	nder
	CDR	Clock and Data Recovery	U
711 .	CTLE	Continuous Time Linear Equalizer	
ed	DDI	Digital Display Interface for DP or HDMI/DVI	
4efil.	DDR3	Third-generation Double Data Rate SDRAM memory technology	
, unc.	DDR3L/RS	DDR3 Low Voltage Reduced Standby Power	
Jundefined undefined un	DDR4/DDR4-RS	Fourth-Generation Double Data Rate SDRAM Memory Technology RS - Reduced Standby Power	
unor	DFE	decision feedback equalizer	
3	DMA	Direct Memory Access	16tilli
	DMI	Direct Media Interface	unos
	DP	DisplayPort*	
- AV	DTS	Digital Thermal Sensor	
d undefined undefined undefined t	eDP*	embedded DisplayPort*	
nder	EU	Execution Unit in the Processor Graphics	
d un.	GSA	Graphics in System Agent	
stines	HDCP	High-bandwidth Digital Content Protection	
nder	HDMI*	High Definition Multimedia Interface	6
dui	IMC	Integrated Memory Controller	stine
	Intel [®] 64 Technology	64-bit memory extensions to the IA-32 architecture	
16 Indefined	Indefin	defines	ed undefined
16 Internet		Datasheet, Volume 1 of 2	
nde.		defil.	
ed u.		unc.	
1 etine		ine ⁰	



Introduction stiffed undefine

ndefined undefined und

Jein	define	sineo	od un-
	ned undefilit	Inder	Aefine
Introduction	INCC	intel ^a	0
Inde		(intel)	/
		d une	
Table 1-2.	Terminology (She	eet 2 of 3)	
d une	Term	Description]
atine	Intel [®] DPST	Intel Display Power Saving Technology	
	Intel [®] PTT	Intel Platform Trust Technology	ed u
	Intel [®] TSX-NI	Intel Transactional Synchronization Extensions	Jefine
	Intel [®] TXT	Intel Trusted Execution Technology	0
ed unde	Intel [®] VT	Intel Virtualization Technology. Processor virtualization, when used in conjunction with Virtual Machine Monitor software, enables multiple, robust independent software environments inside a single platform.	
defined undefined unde	Intel [®] VT-d	Intel Virtualization Technology (Intel VT) for Directed I/O. Intel VT-d is a hardware assist, under system software (Virtual Machine Manager or OS) control, for enabling I/O device virtualization. Intel VT-d also brings robust security by providing protection from errant DMAs by using DMA remapping, a key feature of Intel VT-d.	
efine	IOV	I/O Virtualization	
de	ISP	Image Signal Processor	ed u
	LFM	Low Frequency Mode. corresponding to the Enhanced Intel SpeedStep [®] Technology's lowest voltage/frequency pair. It can be read at MSR CEh [47:40].	define
	LLC	Last Level Cache	IUC.
ind	LPDDR3	Low Power Third-generation Double Data Rate SDRAM memory technology	
Lefined undefined une	LPM	Low-Power Mode. The LPM Frequency is less than or equal to the LFM Frequency. The LPM TDP is lower than the LFM TDP as the LPM configuration limits the processor to single thread operation	
unac	LPSP	Low-Power Single Pipe	-
	LSF	Lowest Supported Frequency. This frequency is the lowest frequency where manufacturing confirms logical functionality under the set of operating conditions.	-
19er	MCP define	Multi Chip Package - includes the processor and the PCH. In some SKUs it might have additional On-Package Cache.	sined !
	MFM	Minimum Frequency Mode. MFM is the minimum ratio supported by the processor and can be read from MSR CEh [55:48].	ndei
	MLC	Mid-Level Cache	0.
sined un	NCTF	Non-Critical to Function. NCTF locations are typically redundant ground or non- critical reserved balls/lands, so the loss of the solder joint continuity at end of life conditions will not affect the overall product functionality.	
	OPC	On-Package Cache	-
d un	PAG	Platform Power Architecture Guide (formerly PDDG)	-
ndefined undefined un	PCH	Platform Controller Hub. The chipset with centralized platform capabilities including the main I/O interfaces along with display connectivity, audio features, power management, manageability, security, and storage features. The PCH may also be referred as "chipset".	ined
	PECI	Platform Environment Control Interface	dern
	PEG	PCI Express Graphics	UI
11.	PL1, PL2, PL3	Power Limit 1, Power Limit 2, Power Limit 3	
	Processor	The 64-bit multi-core component (package)	
ndefined undefined un	Processor Core	The term "processor core" refers to Si die itself, which can contain multiple execution cores. Each execution core has an instruction cache, data cache, and 256-KB L2 cache. All execution cores share the LLC.	
	Processor Graphics	Intel Processor Graphics	
nden	PSR	Panel Self-Refresh	
<i>)</i> /.	Rank	A unit of DRAM corresponding to four to eight devices in parallel, ignoring ECC. These devices are usually, but not always, mounted on a single side of a SODIMM.	etine
	SCI	System Control Interrupt. SCI is used in the ACPI protocol.	inoc
Datasheet, Volun	ne 1 of 2	A undefined undefine	,
od unos		under.	
afine		ned - dunt	





Jed undefined undefined Terminology (Sheet 3 of 3)

UnoTable 1-2. T	Terminology (She		
-	SDP	Description	
	SGX	Scenario Design Power Software Guard Extension	
	SHA	Secure Hash Algorithm	Sint
	SSC	Spread Spectrum Clock	
Jundefined und	Storage Conditions	A non-operational state. The processor may be installed in a platform, in a tray, or loose. Processors may be sealed in packaging or exposed to free air. Under these conditions, processor landings should not be connected to any supply voltages, have any I/Os biased, or receive any clocks. Upon exposure to "free air" (that is, unsealed packaging or a device removed from packaging material), the processor should be handled in accordance with moisture sensitivity labeling (MSL) as indicated on the packaging material.	
0	STR	Suspend to RAM	
	TAC	Thermal Averaging Constant	
	TCC	Thermal Control Circuit	
-	TDP	Thermal Design Power	dein.
-	ТОВ	Tolerance Budget	JUL
10	TTV TDP	Thermal Test Vehicle TDP	
du	V _{CC}	Processor core power supply	
stine	V _{CCGT}	Processor Graphics Power Supply	
	V _{CCIO}	I/O Power Supply	
	V _{CCSA}	System Agent Power Supply	
	V _{CCST}	Vcc Sustain Power Supply	
-	V _{DDQ}	DDR Power Supply	
_	VLD	Variable Length Decoding	10/1
-	VPID	Virtual Processor ID	inos
2	V _{SS}	Processor Ground	

1.8 med ur **Related Documents**

Related Documents (Sheet 1 of 2) Document Number / Location Document 7th Generation Intel[®] Processor Families for U/Y-Platforms Datasheet 334662 Volume 2 of 2 7th Generation Intel[®] Processor Families Specification Update 334663 7th Generation $\text{Intel}^{\textcircled{\text{R}}}$ Processor Families I/O Platform Datasheet Volume 1 of 2 334658 7th Generation Intel[®] Processor Families I/O Platform Datasheet Volume 2 334659 of 2 Advanced Configuration and Power Interface 3.0 http://www.acpi.info/ DDR3L SDRAM Specification http://www.jedec.org LPDDR3 Specification http://www.jedec.org **DDR4** Specification

ned undefined Datasheet, Volume 1 of 2 . . undefined



Introduction stined under the

Table 1-3.

sined undefine	
Introduction Table 1-3. Related Documents (Sheet 2 of 2) Document Embedded DisplayPort* Specification revision 1.4 DisplayPort* Specification revision 1.2	(intel)
Table 1-3. Related Documents (Sheet 2 of 2)	ed unit
Document	
Embedded DisplayPort* Specification revision 1.4	Document Number / Location http://www.vesa.org/ vesa.standards/ http://www.vesa.org/ vesa.standards/
DisplayPort* Specification revision 1.2	http://www.vesa.org/ vesa.standards/
PCI Express* Base Specification Revision 3.0	http://www.pcisig.com/specifi- cations
Intel [®] 64 and IA-32 Architectures Software Developer's Manuals	
tined	ed une
PCI Express* Base Specification Revision 3.0 Intel® 64 and IA-32 Architectures Software Developer's Manuals	ndefilte
Lefineo	Sq ni.
d under inderin	
definec ined b	d ^{ur}
d unden.	define
lefiner ined L	ed une
, under	define
	ed une
under	
sined t	
under	ofineo
tined -	unde.
nder	afineo
ed un	d unde
ndefill	
and unoc	
ndefin	ined
med un	indetti
define.	ined L.
Actimed undefined undefine	unden.
Letine.	ined
d unor inde	//.
retines ined by	-0
4 uno-	efine

undermed underme Datasheet, Volume 1 of 2 .re

Interfaces ned ut

intel red under

2.1 System Memory Interface

- Two channels of DDR3L/-RS, LPDDR3 and DDR4 memory with a maximum of two DIMMs per channel. DDR technologies, number of DIMMs per channel, number of ranks per channel are SKU dependent.
- UDIMM, SO-DIMM, and Memory Down support (based on SKU)
- Single-channel and dual-channel memory organization modes
- Data burst length of eight for all memory organization modes
- DDR3L/-RS I/O Voltage of 1.35V based on Processor Line
- LPDDR3 I/O voltage of 1.2V
- DDR4 I/O Voltage of 1.2V
- 64-bit wide channels
- Non-ECC UDIMM and SODIMM DDR4/DDR3L/-RS support (based on SKU)
- Theoretical maximum memory bandwidth of:
 - 20.8 GB/s in dual-channel mode assuming 1333 MT/s
 - 25.0 GB/s in dual-channel mode assuming 1600 MT/s
 - 29.1 GB/s in dual-channel mode assuming 1866 MT/s
 - 33.3 GB/s in dual-channel mode assuming 2133 MT/s
 - 37.5 GB/s in dual-channel mode assuming 2400 MT/s

undefined ut Note:

2.1.1

led undefiner Memory down of all technologies (DDR3L/DDR4/LPDDR3) should be implemented homogeneously, which means that all DRAM devices should be from the same vendor and have the same part number. Implementing a mix of DRAM devices may cause serious signal integrity and functional issues.

System Memory Technology Supported

The Integrated Memory Controller (IMC) supports DDR3L/-RS, LPDDR3 andDDR4 protocols with two independent, 64-bit wide channels.

Processor DRAM Support Matrix Table 2-1.

unde	Processor Line	DPC ¹	DDR3L/-RS [MT/s]	DDR4 [MT/s]	LPDDR3 [MT/s]
	U-Processor Line	1	1333/1600	1866/2133	1600/1866
	U-Processor Line (U- 4 Core)	1	N/A	2400	1866/2133
red	Y/AML-Y22 Processor Line	1	N/A	N/A	1600/1866
undefined undefined	Notes: 1. DPC = DIMM Per Channel 2. N/A 3. N/A		US.	6~	efined
d undefine	undefine	0.		defined un	
	indefined		defined ut	10	eine
20 Lundefined	undefined undefine	indef	ined undefined un	Da	atasheet, Volume 1 of 2
1 of inec	la in	sq r.		d un	



- undefined undefined undef DDR3L/-RS Data Transfer Rates:
 - 1333 MT/s (PC3-10600)
 - 1600 MT/s (PC3-12800)
 - DDR4 Data Transfer Rates:
 - 1866 MT/s (PC4-1866)
 - 2133 MT/s (PC4-2133)
 - 2400 MT/s (PC4-2400)
 - LPDDR3 Data Transfer Rates:
 - 1600 MT/s
 - 1866 MT/s
 - 2133 MT/s
 - SODIMM Modules:
 - DDR3L/-RS SODIMM/UDIMM Modules:
 - Standard 4-Gb technology and addressing are supported for x8 and x16 devices.

DDR4 SODIMM/UDIMM Modules:

 Standard 4-Gb and 8-Gb technologies and addressing are supported for x8 and x16 devices.

There is no support for memory modules with different technologies or capacities on opposite sides of the same memory module. If one side of a memory module is populated, the other side is either identical or empty.

- DDR3L/-RS Memory Down: Single and dual rank x8, x16 (based on SKU)
- DDR4 Memory Down: Single rank x8, x16 (based on SKU)
- LPDDR3 Memory Down: Single and Dual Rank x32/x64 (based on SKU)

2.1.1.1 DDR3L/-RS Supported Memory Modules and Devices

Table 2-2.

Supported DDR3L/-RS Non-ECC SO-DIMM Module Configurations (U-Processor Line)

lu-	-		emory Modu ECC SO-DIM				5	eined	undefin
	DIMM Capacity		DRAM Organization	# of DRAM Devices	# of Ranks	# of Row/Col Address Bits	# of Banks Inside DRAM	Page Size	
				-		15/10	8	8K	
A	4GB	4Gb	256M x 16	8	2	15/10	0	on	
A B	4GB 4GB	4Gb 4Gb	256M x 16 512M x 8	8	20	16/10	о 8	8K	
					20 1 1		-		defil

Table 2-3.

Supported DDR3L/-RS Memory Down Module Configurations (U-Processor Line) (Sheet 1 of 2)

PKG Type (Dies bits x PKG bits)	Max System Capacity	DRAM Device Technology	DRAM Organization	Die Density	Dies Per Channel	PKGs per channel	# of DRAM Ranks	# of Banks Inside DRAM	Page Size
SDP 8x8	16GB	4Gb	512M x 8	4 Gb	16	16	1	16	8K
SDP 16x16	8GB	4Gb	256M x 16	4 Gb	8	8	1	16	8K
DDP 16x16	8GB	8Gb	256M x 16	4 Gb	8	4	2	16	8K
Datasheet, Volur	me 1 of 2		4 undefine	d under	1.			ned un	define 21
			ed une			6	nuger		



Interfaces

		ndefine			ndefit	1eo			
inte	sheo		20	ndefiner	J. UI.			Ir undef	nterfaces
Table 2-3.					odule Coi	nfiguratio	ensned		
PKG Type (Dies bits x PKG bits)	Max System Capacity	DRAM Device Technology	DRAM Organization	Die Density	Dies Per Channel	PKGs per channel	# of DRAM Ranks	# of Banks Inside DRAM	Page Size
	Table 2-3. PKG Type (Dies bits x	(U-Proc PKG Type Max (Dies bits x System	Table 2-3. Supported DDR3L/ (U-Processor Line) PKG Type (Dies bits x Max System DRAM Device	Table 2-3. Supported DDR3L/-RS Memory (U-Processor Line) (Sheet 2 of PKG Type (Dies bits x Max System DRAM DRAM DRAM Organization	Table 2-3.Supported DDR3L/-RS Memory Down M (U-Processor Line) (Sheet 2 of 2)PKG Type (Dies bits xMax SystemDRAM DeviceDie Density	Table 2-3.Supported DDR3L/-RS Memory Down Module Con (U-Processor Line) (Sheet 2 of 2)PKG Type (Dies bits xMax SystemDRAM DeviceDie DranizationDie DensityDies Per Channel	Table 2-3. Supported DDR3L/-RS Memory Down Module Configuration (U-Processor Line) (Sheet 2 of 2) PKG Type (Dies bits x Max System Device DRAM Die Dies Per Channel Channel Channel	Table 2-3. Supported DDR3L/-RS Memory Down Module Configurations (U-Processor Line) (Sheet 2 of 2) PKG Type (Dies bits x System Device Organization Device Organizatio	Table 2-3. Supported DDR3L/-RS Memory Down Module Configurations (U-Processor Line) (Sheet 2 of 2) PKG Type (Dies bits x (PKG bits)) Max System Canacity DRAM Device Technology DRAM Organization Die Density Dies Per Channel PKGs per Channel # of Banks Inside

Note: Maximum system capacity is referred to 2 channels populated with 2 ranks per channel.

2.1.1.2

DDR4 Supported Memory Modules and Devices

Supported DDR4 Non-ECC SODIMM Module Configurations (U/U-4 Core Processor Line)

	and a und				Jefil'						
	2.1.1.2	DDR4 S	upporte	a memory	Modules a	nd Devic	es		de		
	Table 2-4.			Non-ECC S cessor Line	ODIMM Mode e)	ule Config	guratio	ns	3 UN.		
efined un		Raw Card Version	DIMM Capacity	DRAM Device Technology	DRAM Organization	# of DRAM Devices	# of Ranks	# of Row/Col Address Bits	# of Banks Inside DRAM	Page Size	sined
		A	4GB	4Gb	512M x 8	8	1	15/10	16	8K	dell
		A	8GB	8Gb	1024M x 8	8	1	16/10	16	8K	ULL
	nr.	В	8GB	4Gb	512M x 8	16	2	15/10	16	8K	
	ed u	В	16GB	8Gb	1024M x 8	16	2	16/10	16	8K	
	ndefined und	С	2GB	4Gb	256M x 16	4	1	15/10	8	8K	
, U	no	С	4GB	8Gb	512M x 16	4	1	16/10	8	8K	
ineo		E	8GB	4Gb	512M x 8	16	2	15/10	16	8K	
ein		E	16GB	8Gb	1024M x 8	16	2 0	16/10	16	8K	
		Support	under a	Momory Da	Davisa (Inde	tions				odefine
	Table 2-5.	(U/U-4 (Core Proc	memory Do	own Device ()	Johngura	LIONS				Un

Table 2-5. Supported DDR4 Memory Down Device Configurations (U/U-4 Core Processor Line)

	Max System Capacity	PKG Type (Die bits x PKG bits)	DRAM Organization / PKG Type	PKG Density	Die Density	Die Per Channel	Rank Per Channel	PKGs Per channel	Physical Device Rank	Banks Inside DRAM	Page Size	
21	16GB	SDP 8x8	512M x 8	4Gb	4Gb	16	2	16	1	16	8K	
	32GB	SDP 8x8	1024M x 8	8Gb	8Gb	16	2	16	1	16	8K	
undefined	4GB	SDP 16x16	256M x 16	4Gb	4Gb	4	1	4	1	8	8K	21
Ulli	8GB	SDP 16x16	512M x 16	8Gb	8Gb	4	1 20	4	1	8	8K	
	16GB	DDP 8x16	1024M x 16	16Gb	8Gb	8	1	4	1	16	8K	dell
			em capacity for x8 em capacity for x1								ined	nı.
		2 0			2	UL				nde		

Notes:

The maximum system capacity for x8 devices refers to 2 channels, 2 ranks systems 1. 2. The maximum system capacity for x16 devices refers to 2 channels, 1 rank systems

med undefined Datasheet, Volume 1 of 2



undefined und

LPDDR3 Supported Memory Devices 2.1.1.3

Table 2-6. Supported LPDDR3 x32 DRAMs Configurations (KBL Y/H/U/U-4 Core and AML-Y22 Processor Lines)

					Processo			,		sined u
Max System Capacity	PKG Type (Dies bits x PKG bits)	DRAM Organization / PKG Type	Die Density	PKG Density	Dies Per Channel	PKGs Per Channel	Physical Device Rank	Banks Inside DRAM	Page Size	Idett.
2 GB	SDP 32x32	128Mx32	4 Gb	4Gb	2	2	1	8	8K	
4 GB	DDP 32x32	256Mx32	4 Gb	8Gb	4	2	2	8	8K	
8 GB	QDP 16x32	512Mx32	4 Gb	16Gb	8	2	2 0	8	8K	
4 GB	SDP 32x32	256Mx32	8 Gb	8Gb	2	2	AC'I	8	8K	
8 GB	DDP 32x32	512Mx32	8 Gb	16Gb	4	2 5	2	8	8K	
16 GB	QDP 16x32	1024Mx32	8 Gb	32Gb	8	2	2	8	8K	2

x32 devices are 178 balls. 1

SDP = Single Die Package, DDP = Dual Die Package, QDP = 4 Die Package 2.

Supported LPDDR3 x64 DRAMs Configurations Table 2-7. (KBL Y/U/U-4 Core and AML-Y22 Processor Lines)

							undef		
PKG Type (Dies bits x PKG bits)	DRAM Organization / PKG Type	Die Density	PKG Density	Dies Per Channel	PKGs Per Channel	Physical Device Rank	Banks Inside DRAM	Page Size	
DDP 32x64	128Mx64	4 Gb	8 Gb	2	1	1	8	8K	du
QDP 32x64	256Mx64	4 Gb	16 Gb	4	1	2	8	8K	etine
DDP 32x64	256Mx64	8 Gb	16 Gb	2	1	1	8	8K	inde
QDP 32x64	512Mx64	8 Gb	32 Gb	4	1	2	8	8K 🔿	
	(KBL) PKG Type (Dies bits x PKG bits) DDP 32x64 QDP 32x64 DDP 32x64	(KBL Y/U/U-4 CorePKG Type (Dies bits)DRAM Organization / PKG TypeDDP 32x64128Mx64QDP 32x64256Mx64DDP 32x64256Mx64	(KBL Y/U/U-4 Core and AMIPKG Type (Dies bits)DRAM Organization / PKG TypeDie DensityDDP 32x64128Mx644 GbQDP 32x64256Mx644 GbDDP 32x64256Mx648 Gb	(KBL Y/U/U-4 Core and AML-Y22 ProPKG Type (Dies bits)DRAM Organization PKG TypeDie DensityPKG DensityDDP 32x64128Mx644 Gb8 GbQDP 32x64256Mx644 Gb16 GbDDP 32x64256Mx648 Gb16 Gb	(KBL Y/U/U-4 Core and AML-Y22 Processor LPKG Type (Dies bits)DRAM Organization PKG TypeDie DensityPKG DensityDies Per ChannelDDP 32x64128Mx644 Gb8 Gb2QDP 32x64256Mx644 Gb16 Gb4DDP 32x64256Mx648 Gb2	(KBL Y/U/U-4 Core and AML-Y22 Processor Lines)PKG Type (Dies bits x PKG bits)DRAM Organization / PKG TypeDie DensityPKG DensityDies Per ChannelPKGs Per ChannelDDP 32x64128Mx644 Gb8 Gb21QDP 32x64256Mx644 Gb16 Gb41DDP 32x64256Mx648 Gb16 Gb21	(KBL Y/U/U-4 Core and AML-Y22 Processor Lines)PKG Type (Dies bits x PKG bits)DRAM Organization / PKG TypeDie DensityPKG DensityDies Per ChannelPKGs Per ChannelPhysical Device RankDDP 32x64128Mx644 Gb8 Gb211QDP 32x64256Mx644 Gb16 Gb412DDP 32x64256Mx648 Gb16 Gb211	(KBL Y/U/U-4 Core and AML-Y22 Processor Lines)PKG Type (Dies bits x PKG bits)DRAM Organization / PKG TypeDie DensityPKG DensityDies Per ChannelPKGs Per ChannelPhysical Device RankBanks Inside DRAMDDP 32x64128Mx644 Gb8 Gb2118QDP 32x64256Mx644 Gb16 Gb4128DDP 32x64256Mx648 Gb16 Gb2118	(KBL Y/U/U-4 Core and AML-Y22 Processor Lines)PKG Type (Dies bits x PKG bits)DRAM Organization / PKG TypeDie DensityPKG DensityDies Per ChannelPKGs Per ChannelPhysical Device RankBanks Inside Device RankPage SizeDDP 32x64128Mx644 Gb8 Gb21188KQDP 32x64256Mx644 Gb16 Gb41288KDDP 32x64256Mx648 Gb16 Gb21188K

x64 devices are 253 balls.

SDP = Single Die Package, DDP = Dual Die Package, QDP = 4 Die Package 2.

2.1.2 System Memory Timing Support

The IMC supports the following DDR Speed Bin, CAS Write Latency (CWL), and command signal mode timings on the main memory interface:

- tCL = CAS Latency
- tRCD = Activate Command to READ or WRITE Command delay
- tRP = PRECHARGE Command Period
- CWL = CAS Write Latency
- Command Signal modes:
 - IN indicates a new DDR3L/DDR4 command may be issued every clock
 - 2N indicates a new DDR3L/DDR4 command may be issued every 2 clocks A undefined undefined undefined in a undefined undefined undefined



Table 2-8. **DRAM System Memory Timing Support**

DRAM Sys	stem Memor	sino	Support		afi	ned unde		
DRAM Device	Transfer Rate (MT/s)	tCL (tCK)	tRCD (tCK)	tRP (tCK)	CWL (tCK)	DPC (SODIMM Only)	CMD Mode	d ul
DDR3L/-RS	1333	8/9	8/9	8/9	7	1 or 2	1N/2N	fine
DDR3L/-R5	1600	10/11	10/11	10/11	8	1 or 2	1N/2N	nde.
DDR4	1866	13/14	12/13/14	13/14	10/12/12	1 or 2	1N/2N	0.,
DDR4	2133	15/16	14/15/16	15/16	11/14/14	1 or 2	1N/2N	

ed und Table 2-9.

DRAM System Memory Timing Support (LPDDR3)

DRAM Device	Transfer Rate (MT/s)	tCL (tCK)	tRCD (tCK)	tRPpb ¹ (tCK)	tRPab ² (tCK)	CWL (tCK)
LPDDR3	1600	12	15	15	18	9
LPDDR3	1866	14	17	17	20	11
Notes:	<u>()</u>			70.		

tRPpb = Row Precharge typical time (single bank) 2. tRPab = Row Precharge typical time (all banks)

2.1.3System Memory Organization Modes

The IMC supports two memory organization modes, single-channel and dual-channel. Depending upon how the DDR Schema and DIMM Modules are populated in each memory channel, a number of different configurations can exist.

Single-Channel Mode

In this mode, all memory cycles are directed to a single channel. Single-Channel mode is used when either the Channel A or Channel B DIMM connectors are populated in any order, but not both.

Dual-Channel Mode – Intel[®] Flex Memory Technology Mode

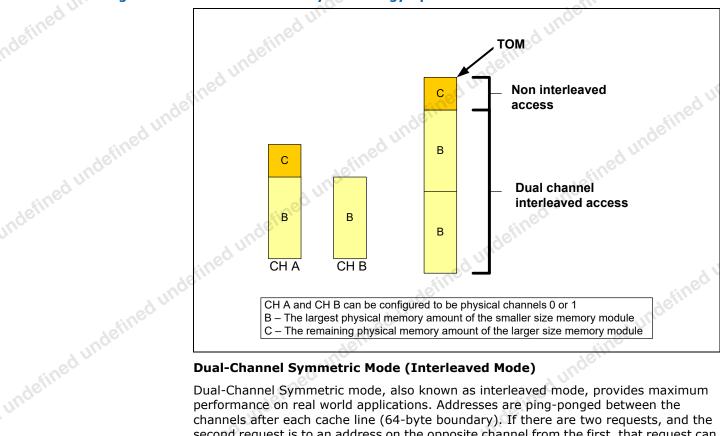
The IMC supports Intel Flex Memory Technology Mode. Memory is divided into a symmetric and asymmetric zone. The symmetric zone starts at the lowest address in each channel and is contiguous until the asymmetric zone begins or until the top address of the channel with the smaller capacity is reached. In this mode, the system in a makelined undefined undefined undefined undefined undefined runs with one zone of dual-channel mode and one zone of single-channel mode, simultaneously, across the whole memory array.

Note:

undefined undefin

Channels A and B can be mapped for physical channel 0 and 1 respectively or vice versa. However, channel A size should be greater or equal to channel B size.





Intel[®] Flex Memory Technology Operations Figure 2-1.

Dual-Channel Symmetric Mode (Interleaved Mode)

Dual-Channel Symmetric mode, also known as interleaved mode, provides maximum performance on real world applications. Addresses are ping-ponged between the channels after each cache line (64-byte boundary). If there are two requests, and the second request is to an address on the opposite channel from the first, that request can be sent before data from the first request has returned. If two consecutive cache lines are requested, both may be retrieved simultaneously, since they are ensured to be on opposite channels. Use Dual-Channel Symmetric mode when both Channel A and Channel B DIMM connectors are populated in any order, with the total amount of memory in each channel being the same.

When both channels are populated with the same memory capacity and the boundary between the dual channel zone and the single channel zone is the top of memory, IMC operates completely in Dual-Channel Symmetric mode.

Note:

Interfaces

The DRAM device technology and width may vary from one channel to the other.

2.1.4System Memory Frequency

In all modes, the frequency of system memory is the lowest frequency of all memory modules placed in the system, as determined through the SPD registers on the memory modules. The system memory controller supports up to two DIMM connectors per channel. If DIMMs with different latency are populated across the channels, the BIOS will use the slower of the two latencies for both channels. For Dual-Channel modes both channels should have a DIMM connector populated. For Single-Channel undefined undefined undefined mode, only a single channel can have a DIMM connector populated. undefined undefined undef



2.1.5

Technology Enhancements of Intel[®] Fast Memory Access (Intel[®] FMA)

The following sections describe the Just-in-Time Scheduling, Command Overlap, and Out-of-Order Scheduling Intel FMA technology enhancements.

Just-in-Time Command Scheduling

The memory controller has an advanced command scheduler where all pending requests are examined simultaneously to determine the most efficient request to be issued next. The most efficient request is picked from all pending requests and issued to system memory Just-in-Time to make optimal use of Command Overlapping. Thus, instead of having all memory access requests go individually through an arbitration mechanism forcing requests to be executed one at a time, they can be started without interfering with the current request allowing for concurrent issuing of requests. This allows for optimized bandwidth and reduced latency while maintaining appropriate command spacing to meet system memory protocol.

Command Overlap

Command Overlap allows the insertion of the DRAM commands between the Activate, Pre-charge, and Read/Write commands normally used, as long as the inserted commands do not affect the currently executing command. Multiple commands can be issued in an overlapping manner, increasing the efficiency of system memory protocol.

Out-of-Order Scheduling

While leveraging the Just-in-Time Scheduling and Command Overlap enhancements, the IMC continuously monitors pending requests to system memory for the best use of bandwidth and reduction of latency. If there are multiple requests to the same open page, these requests would be launched in a back to back manner to make optimum use of the open memory page. This ability to reorder requests on the fly allows the IMC to further reduce latency and increase bandwidth efficiency.

Data Scrambling

The system memory controller incorporates a Data Scrambling feature to minimize the impact of excessive di/dt on the platform system memory VRs due to successive 1s and Os on the data bus. Past experience has demonstrated that traffic on the data bus is not random and can have energy concentrated at specific spectral harmonics creating high di/dt which is generally limited by data patterns that excite resonance between the package inductance and on die capacitances. As a result, the system memory controller uses a data scrambling feature to create pseudo-random patterns on the system memory data bus to reduce the impact of any excessive di/dt.

DDR I/O Interleaving 2.1.7

The processor supports I/O interleaving, which has the ability to swap DDR bytes for routing considerations, BIOS configures the I/O interleaving mode before DDR training.

The KBL Y and AML-Y22 Processor Lines package is optimized only for Non-Interleaving (NIL) mode. in a materined undefined undefined

There are 2 supported modes:

• Interleave (IL)

Datasheet, Volume 1 of 2 -4 undefined

Note:

2.1.6



Non-Interleave (NIL)

undefined undernit

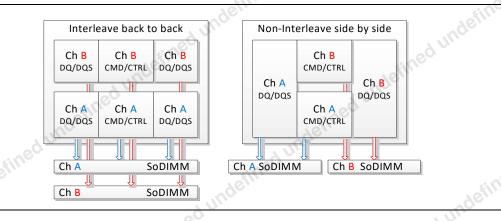
Interfaces

undefined undefined undefined undefined undefined The following table and figure describe the pin mapping between the IL and NIL modes.

ndefined undefined Table 2-10. Interleave (IL) and Non-Interleave (NIL) Modes Pin Mapping

		L	NIL	
defined undefined unde	Channel	Byte	Channel	Byte
inde	DDR0	Byte0	DDR0	Byte0
	DDR0	Byte1	DDR0	Byte1
defill	DDR0	Byte2	DDR0	Byte4
y une	DDR0	Byte3	DDR0	Byte5
	DDR0	Byte4	DDR1	Byte0
dell.	DDR0	Byte5	DDR1	Byte1
	DDR0	Byte6	DDR1	Byte4
	DDR0	Byte7	DDR1	Byte5
A	DDR1	Byte0	DDR0	Byte2
4 Une	DDR1	Byte1	DDR0	Byte3
	DDR1	Byte2	DDR0	Byte6
dein	DDR1	Byte3	DDR0	Byte7
ndefined undefined und	DDR1	Byte4	DDR1	Byte2
atinez	DDR1	Byte5	DDR1	Byte3
	DDR1	Byte6	DDR1	Byte6
	DDR1	Byte7	DDR1	Byte7

Figure 2-2. Interleave (IL) and Non-Interleave (NIL) Modes Mapping



ined un 2.1.8

Data Swapping

By default, the processor supports on-board data swapping in two manners (for all A modefined undefined undefined segments and DRAM technologies):

- byte (DQ+DQS) swapping between bytes in the same channel.
- er and undefined undefined bit swapping within specific byte.

Datasheet, Volume 1 of 2 .ee

undefined un



2.1.9 DRAM Clock Generation

Every supported rank has a differential clock pair. There are a total of four clock pairs driven directly by the processor to DRAM.

2.1.10 DRAM Reference Voltage Generation

The memory controller has the capability of generating the DDR3L/-RS, LPDDR3 and DDR4 Reference Voltage (VREF) internally for both read and write operations. The generated VREF can be changed in small steps, and an optimum VREF value is determined for both during a cold boot through advanced training procedures in order to provide the best voltage to achieve the best signal margins.

2.1.11 Data Swizzling

All Processor Lines does not have die-to-package DDR swizzling.

Processor graphics is not supported on the X-Processor.

2.2 **Processor Graphics**

Note:

The processor graphics is based on Gen 9 LP (generation 9 Low Power) graphics core architecture that enables substantial gains in performance and lower-power consumption over prior generations. Gen 9 LP architecture supports up to 72 Execution Units (EUs) with On-Package Cache depending on the processor SKU.

The processor graphics architecture delivers high dynamic range of scaling to address segments spanning low power to high power, increased performance per watt, support for next generation of APIs. Gen 9 LP scalable architecture is partitioned by usage domains along Render/Geometry, Media, and Display. The architecture also delivers very low-power video playback and next generation analytic and filters for imaging-related applications. The new Graphics Architecture includes 3D compute elements, Multi-format HW assisted decode/encode pipeline, and Mid-Level Cache (MLC) for superior high definition playback, video quality, and improved 3D performance and media.

The Display Engine handles delivering the pixels to the screen. GSA (Graphics in System Agent) is the primary channel interface for display memory accesses and PCI-like traffic in and out.

The display engine supports the latest display standards such as eDP* 1.4, DP* 1.2, HDMI* 1.4, HW support for blend, scale, rotate, compress, high PPI support, and advanced SRD2 display power management.

2.2.1 Operating Systems Support

Windows* 10 x64,OS X, Linux* OS, Chrome* OS.

Note:

The processor supports only 64-bit operating systems.

Datasheet, Volume 1 of 2



s defined unde Interfaces

2.2.2

API Support (Windows*)

- indefined und Direct3D* 2015, Direct3D 11.2, Direct3D 11.1, Direct3D 9, Direct3D 10, Direct2D
- OpenGL* 4.4
- OpenCL* 2.1, OpenCL 2.0, OpenCL 1.2

DirectX* extensions:

PixelSync, InstantAccess, Conservative Rasterization, Render Target Reads, Floating-point De-norms, Shared Virtual memory, Floating Point atomics, MSAA sample-indexing, Fast Sampling (Coarse LOD), Quilted Textures, GPU Enqueue Kernels, GPU Signals processing unit. Other enhancements include color compression.

Gen 9 LP architecture delivers hardware acceleration of Direct X* 11 Render pipeline comprising of the following stages: Vertex Fetch, Vertex Shader, Hull Shader, Tesselation, Domain Shader, Geometry Shader, Rasterizer, Pixel Shader, Pixel Output.

Media Support (Intel[®] OuickSync & Clear Video 2.2.3 Technology HD)

Gen 9 LP implements multiple media video codecs in hardware as well as a rich set of image processing algorithms.

All supported media codecs operate on 8 bpc, YCbCr 4:2:0 video profiles. Note:

2.2.3.1 Hardware Accelerated Video Decode

Gen 9 LP implements a high-performance and low-power HW acceleration for video decoding operations for multiple video codecs.

The HW decode is exposed by the graphics driver using the following APIs:

- Direct3D* 9 Video API (DXVA2)
- Direct3D11 Video API
- Intel Media SDK
- MFT (Media Foundation Transform) filters.

Gen 9 LP supports full HW accelerated video decoding for AVC/VC1/MPEG2/HEVC/VP8/ JPEG.

Table 2-11. Hardware Accelerated Video Decoding (Sheet 1 of 2)

de	Codec	Profile	Level	Maximum Resolution	
MF	PEG2	Main	Main High	1080p	
		Advanced	L3	e ^o	
VC	C1/WMV9	Main	High	3840x3840	
		Simple	Simple	unc	
AV	/C/H264	High Main MVC & stereo	L5.1	2160p(4K)	defined
und me 1	of 2	d un	idefined L.		d undefine
		aned undefined un		od undefined undefine	



ed undefined undefine Table 2-11. Hardware Accelerated Video Decoding (Sheet 2 of 2)

Hardware Accel	erated Video Decodi	ng (Sheet 2 of 2	sined undefine	
Codec	Profile	Level	Maximum Resolution	
VP8	0	Unified level	1080p	
JPEG/MJPEG	Baseline	Unified level	16k x16k	
HEVC/H265 (8 bits)	Main	L5.1	2160(4K)	
HEVC/H265 (10 bits)	Main BT2020, isolate Dec	L5.1	2160(4K)	
VP9	0 (4:2:0 Chroma 8-10bit)	Unified level	2160(4K)	

Expected performance:

More than 16 simultaneous decode streams @ 1080p.

Actual performance depends on the processor SKU, content bit rate, and memory frequency. Hardware decode for H264 SVC is not supported.

Indefined undefined und 2.2.3.2 Hardware Accelerated Video Encode

Gen 9 LP implements a high-performance and low-power HW acceleration for video decoding operations for multiple video codecs.

The HW encode is exposed by the graphics driver using the following APIs:

- Intel Media SDK
- MFT (Media Foundation Transform) filters

undefined undefined Table 2-12. Hardware Accelerated Video Encode

Coc	lec Profile	Level	Maximum Resolution
MPEG2	Main	High	1080p
AVC/H264	High Main	L5.1	2160p(4K)
VP8	Unified profile	Unified level	
JPEG	Baseline	-	16Kx16K
HEVC/H26	5 Main	L5.1	2160p(4K)
VP8 JPEG HEVC/H265 VP9	Support 8 bits 4:2:0 BT2 may be obtained the pre/ processing		

Hardware Accelerated Video Processing 2.2.3.3

There is hardware support for image processing functions such as De-interlacing, Film cadence detection, Advanced Video Scaler (AVS), detail enhancement, image stabilization, gamut compression, HD adaptive contrast enhancement, skin tone enhancement, total color control, Chroma de-noise, SFC pipe (Scalar and Format Conversion), memory compression, Localized Adaptive Contrast Enhancement (LACE), spatial de-noise, Out-Of-Loop De-blocking (from AVC decoder), 16 bpc support for denoise/de-mosaic.

> Datasheet, Volume 1 of 2 -4 undefined



idefined undefined undefined undefined undefined There is support for Hardware assisted Motion Estimation engine for AVC/MPEG2 encode, True Motion, and Image stabilization applications.

fined undefined un The HW video processing is exposed by the graphics driver using the following APIs:

- Direct3D* 9 Video API (DXVA2).
- Direct3D 11 Video API.
- Intel Media SDK.
- MFT (Media Foundation Transform) filters
- Intel CUI SDK.

Note:

Note:

Not all features are supported by all the above APIs. Refer to the relevant documentation for more details.

2.2.3.4 Hardware Accelerated Transcoding

Transcoding is a combination of decode video processing (optional) and encode. Using undefit the above hardware capabilities can accomplish a high-performance transcode pipeline. There is not a dedicated API for transcoding.

The processor graphics supports the following transcoding features:

- Low-power and low-latency AVC encoder for video conferencing and Wireless Display applications.
- Lossless memory compression for media engine to reduce media power.
- HW assisted Advanced Video Scaler.
- Low power Scaler and Format Converter.

Expected performance:

- KBL Y and AML-Y22 Processor Lines: 10x 1080p30 RT (previous generation is 5x 1080p30 RT).
- U/U 4 Core Processor Line: 12x 1080p30 RT (same as previous generation).

Actual performance depends on the processor Line, video processing algorithms used, content bit rate, and memory frequency.

2.2.4 **Camera Pipe Support**

Camera pipe functions such as de-mosaic, white balance, defect pixel correction, black level correction, gamma correction, LGCA, vignette control, Front end Color Space Converter (CSC), Image Enhancement Color Processing (IECP).

2.2.5 Switchable/Hybrid Graphics

The processor supports Switchable/Hybrid graphics.

Switchable graphics: The Switchable Graphics feature allows you to switch between using the Intel integrated graphics and a discrete graphics card. The Intel Integrated Graphics driver will control the switching between the modes. In most cases it will operate as follows: when connected to AC power - Discrete graphic card; when connected to DC (battery) - Intel integrated GFX.

undefined undefined undefined **Hybrid graphics**: Intel integrated graphics and a discrete graphics card work cooperatively to achieve enhanced power and performance.

Datasheet, Volume 1 of 2 etined under



finec

Table 2-13. Switchable/Hybrid Graphics Support

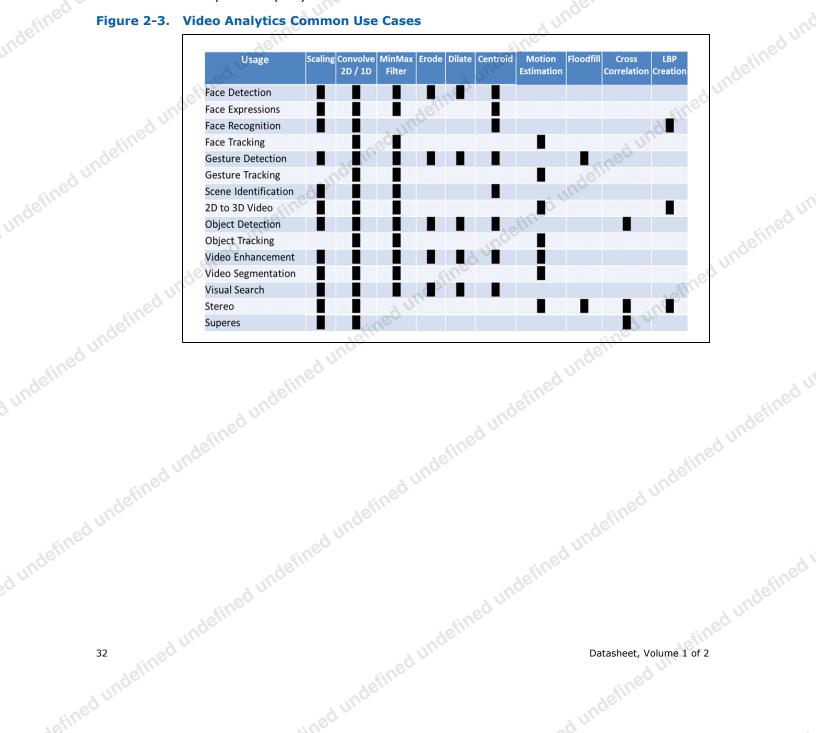
	ed undefinee	Interfac
witchable/Hybrid Graphic	CS Support Hybrid Graphics	Switchable Graphics ²
Windows* 10 (64 bit)	Yes ¹	N/A
Windows* 10 (64 hit)	Yes ¹	N/A

Contact your graphics vendor to check for support. Intel does not validate any SG configurations on Windows* 8.1 or Windows* 10. 2.

2.2.6 **Gen 9 LP Video Analytics**

There is HW assist for video analytics filters such as scaling, convolve 2D/1D, minmax, 1P filter, erode, dilate, centroid, motion estimation, flood fill, cross correlation, Local Binary Pattern (LBP).

indefined undef Figure 2-3. **Video Analytics Common Use Cases**



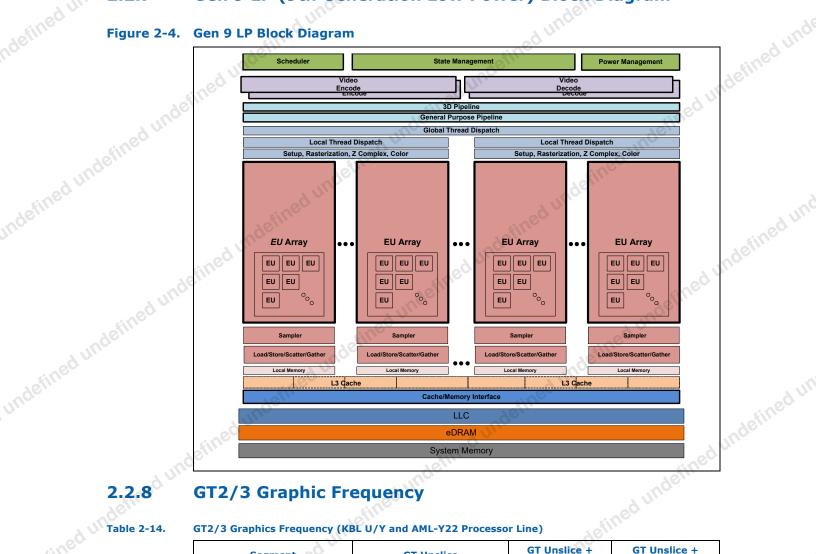
undefined undefined ur



undefined undefined undefi



ndefined undefined undefined undefined ed undefined undefined Gen 9 LP (9th Generation Low Power) Block Diagram



Gen 9 LP Block Diagram

2.2.8

GT2/3 Graphic Frequency

Table 2-14.

GT2/3 Graphics Frequency (KBL U/Y and AML-Y22 Processor Line)

	· · · · · · · · · · · · · · · · · · ·				-
undefineo	Segment	GT Unslice	GT Unslice + 1 GT Slice	GT Unslice + 2 GT Slice	_ V
UNT	Y-Processor Line and AML Y- Processor Line- 2 Core with GT2	GT Max Dynamic frequency	[GT Unslice only] - (1or2)BIN	-	odefineo
	U-Processor Line- 2 Core with GT2	GT Max Dynamic frequency	[GT Unslice only] - (1or2)BIN	-	d UN
ed un	U-Processor Line- 2 Core with GT3 and OPC	GT Max Dynamic frequency	[GT Unslice only] - (1or2)BIN	[GT Unslice + 1 Slice] - (1or2)BIN	
define	U-Processor Line - 4 Core with GT2 (U-4 Core)	GT Max Dynamic frequency	[GT Unslice only] - (1or2)BIN	ned un	
d undefined undefined un	fined undefined un	-8 ¹	Indefined unde		undefined
Datasheet, Volum	le 1 of 2	ndefined undefined u		efined undefine	3
10fint	sineo -		dun.		

undefined un

intel) ed undef

Display Interfaces

The processor supports single eDP* interface and 2 DDI interfaces (depends on segment):

- DDI interface can be configured as DisplayPort* or HDMI*.
- Each DDI can support dual mode (DP++).
- Each DDI can support DVI (DVI max resolution is 1920x1200 @ 60 Hz).
- The DisplayPort* can be configured to use 1, 2, or 4 lanes depending on the bandwidth requirements and link data rate.
- DDI ports notated as: DDI B, C, D.
- Y-Processor /AML-Y22 Processor and U/U- 4 Core Processors support eDP and up to 2 DDI supporting DP/HDMI.
- AUX/DDC signals are valid for each DDI Port. (Two for U/Y and U- 4 Core Processors)
- Total Five dedicated HPD (Hot plug detect signals) are valid for all processor SKUs.

Note:

Note:

The processor platform supports DP Type-C implementation with additional discrete components.

Table 2-15. VGA and Embedded DisplayPort* (eDP*) Bifurcation Summary

SSC is supported in eDP*/DP for all Processor Lines.

Port	U/Y-Processor Line
eDP - DDIA (eDP lower x2 lanes, [1:0])	N/A
VGA - DDIE ² (DP upper x2 lanes, [3:2])	N/A
Notes:	Yeur, sine

2. DP-to-VGA converter on the processor ports is supported using external dongle only, display driver software for VGA dongles which configures the VGA port as a DP branch device.

The technologies supported by the processor are listed in the following table.

ndefined unde Table 2-16. Embedded DisplayPort (eDP*)/DDI Ports Availability (Sheet 1 of 2)

Table 2-16.	Embedded Disp	olayPort (eDP*)/	DDI Ports Availability (Sheet 1 of 2)	
UNO	Ports	Port Name in VBT	U/U-Quad Core/Y-Processor Line ^{2,3}	sined c
С ^р	DDI0 - eDP	Port A	Yes	dell
	DDI1	Port B	Yes	dun
č., .	DDI2	Port C	Yes	AINE
ed v	DDI3	Port D	No ⁴	der.
40fille	DDI4 - eDP/VGA	Port E	No	
ed undefined undefined u	und und	efined L	thed undefined unc	dundefined
ad undefined undefined	INOC	roed undefin	ed undefined undefined undefined Datasheet, Volu	me 1 of 2

Table 2-16. Embedded DisplayPort (eDP*)/DDI Ports Availability (Sheet 2 of 2)

	Ports	Port Name in VBT	U/U-Quad Core/Y-Processor Line ^{2,3}	24
F	Notes:		d'u.	- uno.
	 Port E is bifure 	cated from eDP, when V	GA is used need to use available AUX (if HDMI is in used).	
	shoul	d be used as DDPE_HPD		fine
	3xDDC (DDPB	, DDPC, DDPD) are vali	d for all the processor SKUs (for U/Y and U-Quad Core Processor	196.
	Line DDC sign	als description, refer to	the PCH Datasheet) (See Related Document section).	
	3. 5xHPD (PCH)	inputs (eDP_HPD, DDPE	B_HPD0, DDPC_HPD1, DDPD_HPD2, DDPE_HPD3) are valid for all	

processor SKUs.

undefined undermi

Interfaces

- 4 No Port D for Y/U- and U-Quad Core -Processor Line. DDI3_AUX are exists as reserved.
- VBT provides a configuration option to select the four AUX channels A/B/C/D for a given port, based on 5. how the aux channel lines are connected physically on the board.

Indefined undefined unde Table 2-17. Display Technologies Support

	Display recline	Jogles Support	
lefines	Technology	Standard	, ind
INGE	eDP* 1.4	VESA* Embedded DisplayPort* Standard 1.4	edu
	DisplayPort* 1.2	VESA DisplayPort* Standard 1.2 VESA DisplayPort* PHY Compliance Test Specification 1.2 VESA DisplayPort* Link Layer Compliance Test Specification 1.2	ndefine
60	HDMI* 1.4 ¹	High-Definition Multimedia Interface Specification Version 1.4	
4 undefined u.	supports 2 mo a. Level	a support is possible using LS-Pcon converter chip connected to the DP port. The LS-Pcon des: shifter for HDMI 1.4 resolutions. MI 2.0 protocol converter for HDMI 2.0 resolutions.	
adefined	• The HDMI* i x.v.Color.	nterface supports HDMI with 3D, 4Kx2K @ 24 Hz, Deep Color, and	d un
U		or supports High-bandwidth Digital Content Protection (HDCP) for high ntent playback over digital interfaces. HDCP is not supported for eDP.	definee

- DP-HDMI 2.0 protocol converter for HDMI 2.0 resolutions. b.
- The HDMI* interface supports HDMI with 3D, 4Kx2K @ 24 Hz, Deep Color, and x.v.Color.
- The processor supports High-bandwidth Digital Content Protection (HDCP) for high definition content playback over digital interfaces. HDCP is not supported for eDP.
- The processor supports eDP display authentication: Alternate Scrambler Seed Reset (ASSR).
- The processor supports Multi-Stream Transport (MST), enabling multiple monitors to be used via a single DisplayPort connector.

The maximum MST DP supported resolution for U/U-4 Core/Y-Processors is shown in the following table. ined undefined u

undefined undefined Table 2-18. Display Resolutions and Link Bandwidth for Multi-Stream Transport Calculations (Sheet 1 of 2)

		-				- 10 ¹
	Pixels per line	Lines	Refresh Rate [Hz]	Pixel Clock [MHz]	Link Bandwidth [Gbps]	d under.
711	640	480	60	25.2	0.76	inec
undefined undefined un	800	600	60	40	1.20	
Lefine .	1024	768	60	65	1.95	
Inde	1280	720	60	74.25	2.23	
ed V	1280	768	60	68.25	2.05	
afine	1360	768	60	85.5	2.57	
nde	1280	1024	60	108	3.24	, 6°
d V.	1400	1050	60	101	3.03	fine
	1680	1050	60	119	3.57	nde
, un	defitt		defi	nec		of ined undefined i
Datasheet, Volume	1 of 2		d Ulli			35
roed underth		d undefit			indefined und	
10fill		eineu			9 v.	

intel ned underme

ed undefined underined Table 2-18. Display Resolutions and Link Bandwidth for Multi-Stream Transport Calculations (Sheet 2 of 2)

d un	Calculations (Sheet 2 of 2)			defili		
odefined un	Pixels per line	Lines	Refresh Rate [Hz]	Pixel Clock [MHz]	Link Bandwidth [Gbps]	d undefined und
	1920	1080	60	148.5	4.46	sineu
	1920	1200	60	154	4.62	dell
	2048	1152	60	156.75	4.70	d Une
	2048	1280	60	174.25	5.23	0e0
indefined undefined und	2048	1536	60	209.25	6.28	
	2304	1440	60	218.75	6.56	
dell	2560	1440	60	241.5	7.25	
A UIL	3840	2160	30	262.75	7.88	
	2560	1600	60	268.5	8.06	
delli	2880	1800	60	337.5	10.13	
	3200	2400	60	497.75	14.93	sineu
	3840	2160	60	533.25	16.00	detti
	4096	2160	60	556.75	16.70	d undefined un
	4096	2304	60	605	18.15	neo
red un	Notes:	ed to bit depth of 2	nde.		nde	Inc

Notes

- The data rate for a given video mode can be calculated as: Data Rate = Pixel Frequency * Bit 2. Depth.
- 3. The bandwidth requirements for a given video mode can be calculated as: Bandwidth = Data Rate * 1.25 (for 8B/10B coding overhead).

The Table above is partial List of the common Display resolutions, just for example. The Link Bandwidth depends if the standards is Reduced Blanking or not. 4. If the Standard is Not reduced blanking, the expected Bandwidth will be higher.

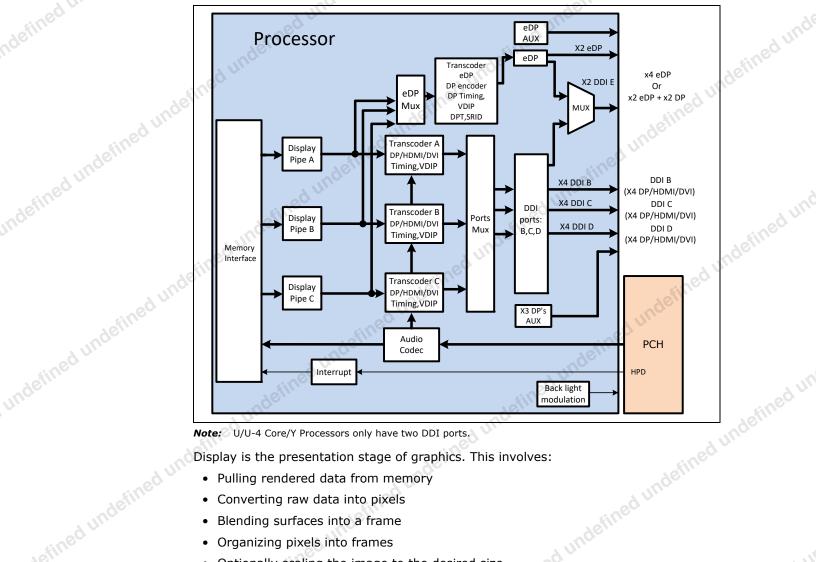
For more details, refer to VESA and Industry Standards and Guidelines for Computer Display Monitor Timing (DMT), Version 1.0, Rev. 13 February 8, 2013

- To calculate the resolutions that can be supported in MST configurations, follow the below 5. guidelines:
 - а. Identify what is the Link Bandwidth (column right) according the requested Display resolution.
 - Summarize the Bandwidth for Two of three Displays accordingly, and make sure the final result is below 21.6Gbps. (for HBR2, four lanes) For special cases when x2 lanes are used or HBR or RBR used, refer to the tables in Section 2.3.11, "Display Resolution per Link Width" accordingly. b.
 - с. For examples:
 - - Docking Two displays: 3840x2160 @ 60 Hz + 1920x1200 @ 60 Hz = 16 + 4.62 = 20.62 Gbps [Supported] a.
- undefined undefined un b. Docking Three Displays: 3840x2160 @ 30 Hz + 3840x2160 @ 30 Hz + 1920x1080 @ 60 Hz = 7.88 + 7.88 + 4.16 = 19.92 Gbps [Supported]
 Consider also the supported resolutions as mentioned in Section 2.3.6, "Multiple Display 6. Configurations (Dual Channel DDR)" and Section 2.3.7, "Multiple Display Configurations (Single Channel DDR)
 - The processor supports only 3 streaming independent and simultaneous display combinations of DisplayPort*/eDP*/HDMI/DVI monitors. In the case where 4 monitors are plugged in, the software policy will determine which 3 will be used.
 - Three High Definition Audio streams over the digital display interfaces are supported.
 - For display resolutions driving capability, see Maximum Display Resolution table.
 - DisplayPort* Aux CH supported by the processor, while DDC channel, Panel power sequencing, and HPD are supported through the PCH. , ai

Datasheet, Volume 1 of 2 -4 undefined

undefined undefined unt

(intel)



led undefined undefined Figure 2-5. Processor Display Architecture (with 3 DDI ports as an example)

Note: U/U-4 Core/Y Processors only have two DDI ports.

Display is the presentation stage of graphics. This involves:

- Pulling rendered data from memory
- Converting raw data into pixels
- Blending surfaces into a frame
- Organizing pixels into frames
- Optionally scaling the image to the desired size
- Re-timing data for the intended target
- Formatting data according to the port output standard

undefined undefinit

Interfaces

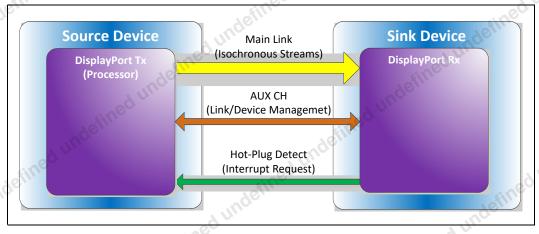
...ig dat. rormatting dat ...1 DisplayPort* The DisplayPort* achieve a and The DisplayPort* is a digital communication interface that uses differential signaling to achieve a high-bandwidth bus interface designed to support connections between PCs and monitors, projectors, and TV displays.

A undefined undefined undefined A DisplayPort* consists of a Main Link, Auxiliary channel, and a Hot-Plug Detect signal. The Main Link is a unidirectional, high-bandwidth, and low-latency channel used for transport of isochronous data streams such as uncompressed video and audio. The

Auxiliary Channel (AUX CH) is a half-duplex bidirectional channel used for link management and device control. The Hot-Plug Detect (HPD) signal serves as an interrupt request for the sink device.

The processor is designed in accordance to VESA* DisplayPort* specification. Refer to Table 2-17, "Display Technologies Support".





2.3

High-Definition Multimedia Interface (HDMI*)

The High-Definition Multimedia Interface (HDMI*) is provided for transmitting uncompressed digital audio and video signals from DVD players, set-top boxes, and other audio-visual sources to television sets, projectors, and other video displays. It can carry high-quality multi-channel audio data and all standard and high-definition consumer electronics video formats. The HDMI display interface connecting the processor and display devices uses transition minimized differential signaling (TMDS) to carry audiovisual information through the same HDMI cable.

HDMI includes three separate communications channels: TMDS, DDC, and the optional CEC (consumer electronics control). CEC is not supported on the processor. As shown in the following figure, the HDMI cable carries four differential pairs that make up the TMDS data and clock channels. These channels are used to carry video, audio, and auxiliary data. In addition, HDMI carries a VESA DDC. The DDC is used by an HDMI Source to determine the capabilities and characteristics of the Sink.

Audio, video, and auxiliary (control/status) data is transmitted across the three TMDS data channels. The video pixel clock is transmitted on the TMDS clock channel and is used by the receiver for data recovery on the three data channels. The digital display data signals driven natively through the PCH are AC coupled and needs level shifting to convert the AC coupled signals to the HDMI compliant digital signals.

The processor HDMI interface is designed in accordance with the High-Definition weined undefined undefined undefined undefined un Multimedia Interface.

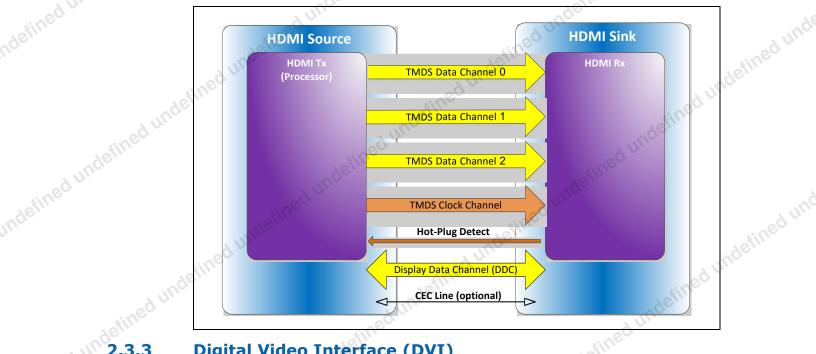
Datasheet, Volume 1 of 2



Figure 2-7. **HDMI*** Overview

s defined under

Interfaces



2.3.3

Digital Video Interface (DVI)

The processor Digital Ports can be configured to drive DVI-D. DVI uses TMDS for transmitting data from the transmitter to the receiver, which is similar to the HDMI through the processor are AC coupled and need level shifting to convert the AC coupled signals to the HDMI compliant digital signals.

2.3.4

embedded DisplayPort* (eDP*)

The embedded DisplayPort* (eDP*) is an embedded version of the DisplayPort standard oriented towards applications, such as notebook and All-In-One PCs. Like DisplayPort, embedded DisplayPort* also consists of a Main Link, Auxiliary channel, and red undefined u an optional Hot-Plug Detect signal.

2.3.5 **Integrated Audio**

- HDMI* and display port interfaces carry audio along with video.
- The processor supports 3 High Definition audio streams on 3 digital ports simultaneously (the DMA controllers are in the PCH).
- The integrated audio processing (DSP) is performed by the PCH, and delivered to the processor using the AUDIO SDI and AUDIO CLK inputs pins.
- AUDIO_SDO output pin is used to carry responses back to the PCH.
- in a materined undefined undefine Supports only the internal HDMI and DP CODECs.



Table 2-19. Processor Supported Audio Formats over HDMI and DisplayPort

Audio Formats	HDMI*	DisplayPort*
AC-3 Dolby* Digital	Yes	Yes
Dolby Digital Plus	Yes	Yes
DTS-HD*	Yes	Yes
LPCM, 192 kHz/24 bit, 8 Channel	Yes	Yes
Dolby TrueHD, DTS-HD Master Audio* (Lossless Blu-Ray Disc* Audio Format)	Yes	Yes

defined undefined und The processor will continue to support Silent stream. Silent stream is an integrated audio feature that enables short audio streams, such as system events to be heard over the HDMI* and DisplayPort* monitors. The processor supports silent streams over the HDMI and DisplayPort interfaces at 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, and 192 kHz sampling rates.

2.3.6 Multiple Display Configurations (Dual Channel DDR)

The following multiple display configuration modes are supported (with appropriate driver software):

- Single Display is a mode with one display port activated to display the output to one display device.
- Intel Display Clone is a mode with up to three display ports activated to drive the display content of same color depth setting but potentially different refresh rate and resolution settings to all the active display devices connected.
- Extended Desktop is a mode with up to three display ports activated to drive the content with potentially different color depth, refresh rate, and resolution settings on each of the active display devices connected.

The digital ports on the processor can be configured to support DisplayPort/HDMI/DVI. The following table shows examples of valid three display configurations through the processor.

Table 2-20. Maximum Display Resolution (Sheet 1 of 2)

ad t			- /	<u> </u>	7
Jefined	Standard	Y-Processor Line	U/U-Quad Core Processor Line	Notes	20
	eDP*	2880x1800 @ 60Hz, 24bpp Or 3840x2160 @ 60Hz, 24bpp ⁴	3840x2160 @ 60Hz, 24bpp ⁴ Or 4096x2304 @ 60Hz, 24bpp ⁴	1,2,3,7	Jefined Undefined U
du	DP*	2880x1800 @ 60Hz, 24bpp Or 3840x2160 @ 60Hz, 24bpp ⁴	3840x2160 @ 60Hz, 24bpp ⁴ Or 4096x2304 @ 60Hz, 24bpp ⁴	1,2,3,7	defined
odefine	HDMI* 1.4 (native)	4096x2160 @ 30 Hz, 24bpp ⁴	4096x2160 @ 30 Hz, 24bpp ⁴	1,2,3	une
defined undefined u	HDMI 2.0/2.0a (Via LS-Pcon)	2880x1800 @ 60Hz, 24bpp Or 3840x2160 @ 60Hz, 24bpp ⁴	3840x2160 @ 60Hz, 24bpp ⁴ Or 4096x2160 @ 60Hz, 24bpp ⁴	1,2,3,6	
		ed undefined u	defined undefine		tined undefined
40 Hotined		undefined	na	Datasheet,	Volume 1 of 2
1 etine		ined "	, in the second s	unt	

ed undefined undefined u



d undefined undefine Table 2-20. Maximum Display Resolution (Sheet 2 of 2)

Standard Y-Processor	e U/U-Quad Core Processor Line Notes
Notes:	

Maximum resolution is based on implementation of 4 lanes with HBR2 link data rate. bpp - bit per pixel. N/A

- 2. 3.
- 4. N/A

undefined undemm

Interfaces

- In the case of connecting more than one active display port, the processor frequency may 5. be lower than base frequency at thermally limited scenario.
- HDMI2.0 implemented using LSPCON device. Only one LSPCON with HDCP2.2 support is 6. supported per platform.
- 7. Display resolution of 5120x2880@60Hz can be supported with 5K panels displays which have two ports. (with the GFX driver accordingly).

Indefined undefined unde Multiple Display Configurations (Single Channel DDR)

Y/AML Y22-Processor Lines Display Resolution Configuration

.3.7 Multiple Di able 2-21. Y/AML Y22-Pr	(e ⁰	Irations (Single (01.	fined
ined th	Maximu	m Resolution (Clone/ Exten	ded mode)	inder
Minimum DDR speed [MT/s]	eDP @ 60 Hz (Primary)	DP @ 60 Hz / HDMI @ 30 Hz (Secondary 1)	DP @ 60 Hz / HDMI @ 30 Hz (Secondary 2)	ed r.
neo -	2880 x 1800 🔊	Not Connected	Not Connected	
1333	2880 x 1800	2880 x 1800	Not Connected	1
	2880 x 1800	2880 x 1800	2880 x 1800	

Table 2-22. U/U-4 Core Processor Lines Display Resolution Configuration

Note: This resolution is limited by	power.		unos	
able 2-22. U/U-4 Core	Processor Lines Di	splay Resolution Config	guration	stined
ined -	Maximu	Im Resolution (Clone/ Extend	ded mode)	inde.
Minimum DDR speed [MT/s]	eDP @ 60 Hz (Primary)	DP @ 60 Hz / HDMI @ 30 Hz (Secondary 1)	DP @ 60 Hz / HDMI @ 30 Hz (Secondary 2)	led L
1222	3840 x 2160	Not Connected	Not Connected	
1333	3200 x 1800	3840 x 2160	Not Connected	
1600	3840 x 2160	3840 x 2160	Not Connected	
1600	2560 x 1440	3840 x 2160	3840 x 2160	
1866	3200 x 1800	3840 x 2160	3840 x 2160	-
2133	3840 x 2160	3840 x 2160	3840 x 2160	60
2400	3840 x 2160	3840 x 2160	3840 x 2160	- fine

Table 2-23. U/U- 4 Core Processor Lines Display Resolution Configuration (DP @ 30 Hz) (Sheet 1 of 2)

			20	<u> </u>	
	red	Maximum			
1	Minimum DDR speed [MT/s]	eDP @ 60 Hz (Primary)	DP @ 30 Hz (Secondary 1)	DP @ 30 Hz (Secondary 2)	
		3840 x 2160	Not Connected	Not Connected	
adefined	1333	3840 x 2160	3840 x 2160	Not Connected	
unos	5.	3200 x 1800	3840 x 2160	3840 x 2160	ed)
	1600 ¹	3840 x 2160	3840 x 2160	3840 x 2160	defill
	Datasheet, Volume 1 of 2		undefined	de	ined unc
i efined	undefine	ined undefined		d undefined un	

Jundefined ur



intel red under

Table 2-23. U/U- 4 Core Processor Lines Display Resolution Configuration (DP @ 30 Hz) (Sheet 2 of 2)

Minimum DDR speed [MT/s]	Maximum Resolution (Clone/ Extended mode)				
	eDP @ 60 Hz (Primary)	DP @ 30 Hz (Secondary 1)	DP @ 30 Hz (Secondary 2)		
Note:		7 01.			

1. eDP with 3840x2160 @ 60 Hz resolution is very close to maximum limit and may not be supported for U/U-4 Core Processor Line.

2.3.8 High-bandwidth Digital Content Protection (HDCP)

HDCP is the technology for protecting high-definition content against unauthorized copy or unreceptive between a source (computer, digital set top boxes, and so on) and the sink (panels, monitor, and TVs). The processor supports HDCP 2.2 for 4k Premium content protection over wired displays (HDMI*, DVI, and DisplayPort*).

The HDCP 2.2 keys are integrated into the processor and customers are not required to physically configure or handle the keys. HDCP2.2 for HDMI2.0 is covered by the LSPCON platform device.

Some minor difference will be between Integrated HDCP2.2 over HDMI1.4 compared to the HDCP2.2 over LSPCON in HDMI1.4 Mode. Also, LSPCON is needed for HDMI 2.0a which defines HDR over HDMI.

The HDCP 1.4 keys are integrated into the processor and customers are not required to physically configure or handle the keys.

Table 2-24		ally configur Display su			eys. ations Table	Lefined unde	ined ut
Торіс	HDCP Revision	Maximum Resolution	HDR ¹	HDCP Solution ²	BPC ³	Comments	unden.
22	HDCP1.4	4K@60	No	iHDCP	10 bit	Legacy Integrated for HDCP1.4	0.
DP	HDCP2.2	4K@60	Yes	iHDCP	10 bit	New Integrated for HDCP2.2	
fille	HDCP1.4	4K@30	No	iHDCP	8 bit	Legacy Integrated for HDCP1.4	
HDMI1.4	HDCP2.2	4K@30	No	LSPCON	8 bit	LSPCON HDCP2.2 required	
ь. Г	HDCP2.2	4K@30	No	iHDCP ⁴	8 bit	New Integrated for HDCP2.2	
HDMI2.0	HDCP2.2	4K@60	No	LSPCON	12 bit (YUV 420)	LSPCON HDCP2.2 required	
HDMI2.0a	HDCP2.2	4K@60	Yes	LSPCON	12 bit (YUV 420)	LSPCON HDCP2.2 required	ed '
M - 6						201	11:5

undefined undefined Table 2-24. HDCP Display supported Implications Table

Notes:

HDR - High Dynamic Range feature expands the range of both contrast and color significantly, HDR will be supported on DP and HDMI2.0a configuration only.

2. HDCP Solutions:

- iHDCP Intel Silicon Integrated HDCP a.
- LSPCon 3rd Party motherboard soldered down solution h
- 3. BPC - Bits Per Channel.
- HDMI1.4 with the Integrated HDCP2.2 solution will replace the LSPCON Solution at a later time. 4.
- HDCP2.2 is supported by KBL U/Y and AML Y22-Processors with integrated HDCP2.2 and by U-Processors 2+3e. HDCP2.2 is 5. not supported by Y/U-Processors without integrated HDCP2.2. undefined undefined undefined

Datasheet, Volume 1 of 2 -4 undefined



Display Link Data Rate Support 2.3.9

Table 2-25. Display Link Data Rate Support

	Technology	Link Data Rate	efin
	- d 011	RBR (1.62 GT/s)	inoc
	in ^e	2.16 GT/s	-9.0
	e l'	2.43 GT/s	
	eDP*	HBR (2.7 GT/s)	
4 V.		3.24 GT/s	
		4.32 GT/s	
deim		HBR2 (5.4 GT/s)	
unc		RBR (1.62 GT/s)	
	DisplayPort*	HBR (2.7 GT/s)	
		HBR2 (5.4 GT/s)	
	HDMT*	1.65 Gb/s	
	HDMI*	2.97 Gb/s	

Table 2-26. Display Resolution and Link Rate Support

Resolution	Link Rate Support	High Definition
4096x2304	5.4 (HBR2)	O UHD (4K)
3840x2160	5.4 (HBR2)	UHD (4K)
3200x2000	5.4 (HBR2)	QHD+
3200x1800	5.4 (HBR2)	QHD+
2880x1800	2.7 (HBR)	QHD
2880x1620	2.7 (HBR)	QHD
2560x1600	2.7 (HBR)	QHD
2560x1440	2.7 (HBR)	QHD
1920x1080	1.62 (RBR)	FHD

2.3.10 **Display Bit Per Pixel (BPP) Support**

Table 2-27. Display Bit Per Pixel (BPP) Support

Technology	Bit Per Pixel (bpp)
eDP*	24,30,36
DisplayPort*	24,30,36
HDMI*	24,36

2.3.11 **Display Resolution per Link Width**

Table 2-28. Supported Resolutions¹ for HBR (2.7 Gbps) by Link Width (Sheet 1 of 2)

Link Width	Max Link Bandwidth [Gbps]	Max Pixel Clock (theoretical) [MHz]	U/Y-Processor Lines	
4 lanes	10.8	360	2880x1800 @ 60 Hz, 24bpp	the Contraction of the Contracti
2 lanes	5.4	180	2048x1280 @ 60 Hz, 24bpp	defini
ne 1 of 2	ined undefined ut	ndefineo	d undefined undefine	3 3

Datasheet, Volume 1 of 2 uneined undel



Table 2-28. Supported Resolutions¹ for HBR (2.7 Gbps) by Link Width (Sheet 2 of 2)

Link Width	Max Link Bandwidth [Gbps]	Max Pixel Clock (theoretical) [MHz]	U/Y-Processor Lines	
1 lane	2.7	90	1280x960 @ 60 Hz, 24bpp	

Notes:

The examples assumed 60 Hz refresh rate and 24 bpp. 1.

Supported Resolutions¹ for HBR2 (5.4 Gbps) by Link Width Table 2-29.

Supported Resolutions ¹ for HBR2 (5.4 Gbps) by Link Width						
Link Width	Max Link Bandwidth [Gbps]	Max Pixel Clock (theoretical) [MHz]	U/Y-Processor Lines			
4 lanes	21.6	720	See "Maximum Display Resolutions" table			
2 lanes	10.8	360	2880x1800 @ 60 Hz, 24bpp			
1 lane	5.4	180	2048x1280 @ 60 Hz, 24bpp			
Notes:		1etti				

The examples assumed 60 Hz refresh rate and 24 bpp. 1. 2.

undefined undefined 2.4

Platform Environmental Control Interface (PECI)

PECI is an Intel proprietary interface that provides a communication channel between Intel processors and external components like Super IO (SIO) and Embedded Controllers (EC) to provide processor temperature, Turbo, Configurable TDP, and memory throttling control mechanisms and many other services. PECI is used for platform thermal management and real time control and configuration of processor features and performance.

2.4.1 **PECI Bus Architecture**

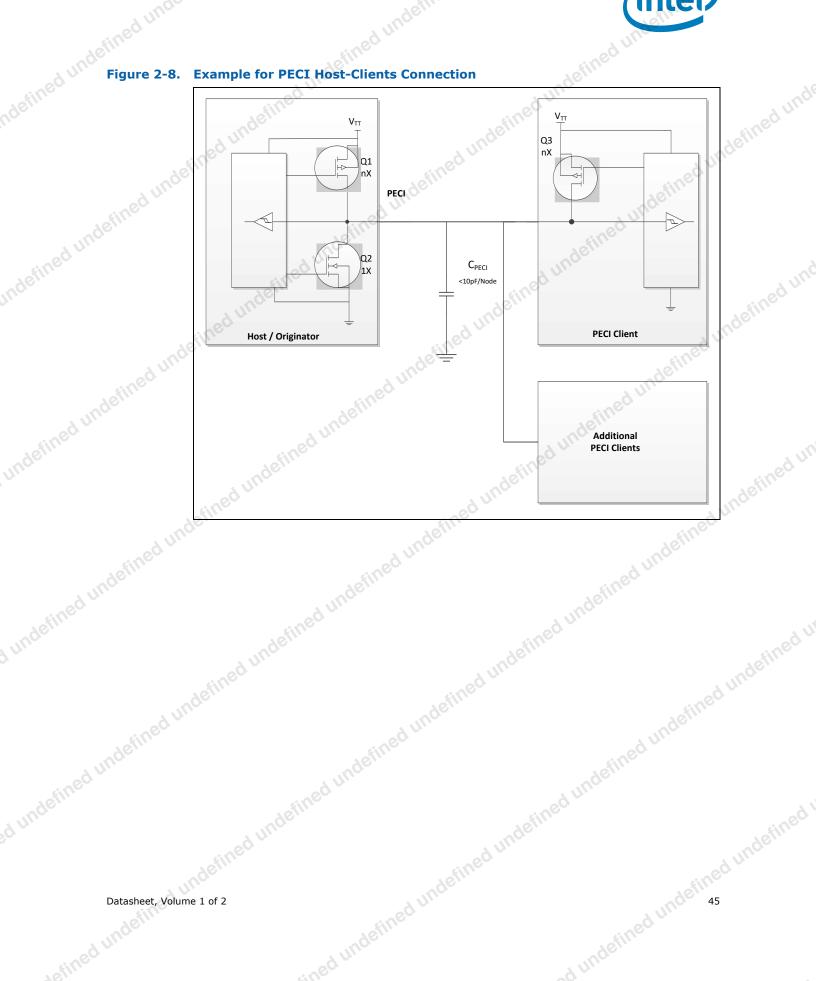
The PECI architecture is based on a wired OR bus that the clients (as processor PECI) can pull up (with strong drive).

The idle state on the bus is near zero.

The following figures demonstrates PECI design and connectivity:

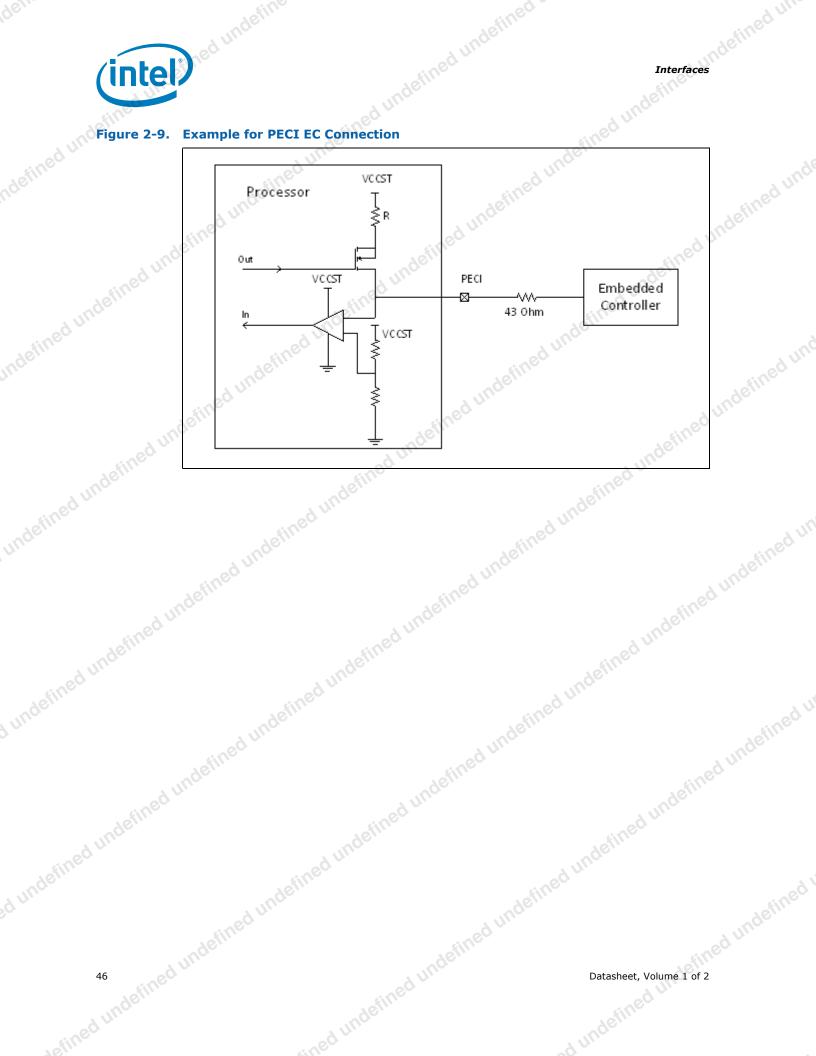
- PECI Host-Clients Connection: While the host/originator can be third party PECI host and one of the PECI client is a processor PECI device.
 - PECI EC Connection.





undefined underme

Interfaces



3.1



Technologies

This chapter provides a high-level description of Intel technologies implemented in the processor.

The implementation of the features may vary between the processor SKUs.

Details on the different technologies of Intel processors and other relevant external notes are located at the Intel technology web site: http://www.intel.com/technology/

Intel[®] Virtualization Technology (Intel[®] VT)

Intel[®] Virtualization Technology (Intel[®] VT) makes a single system appear as multiple independent systems to software. This allows multiple, independent operating systems to run simultaneously on a single system. Intel VT comprises technology components to support virtualization of platforms based on Intel architecture microprocessors and chipsets.

Intel Virtualization Technology (Intel VT) for IA-32, Intel 64 and Intel Architecture (Intel VT-x) added hardware support in the processor to improve the virtualization performance and robustness. Intel Virtualization Technology for Directed I/O (Intel VTd) extends Intel VT-x by adding hardware assisted support to improve I/O device virtualization performance.

Intel VT-x specifications and functional descriptions are included in the Intel 64 and IA-32 Architectures Software Developer's Manual, Volume 3. Available at:

http://www.intel.com/products/processor/manuals/index.htm

The Intel VT-d specification and other VT documents can be referenced at:

http://www.intel.com/technology/virtualization/index.htm

https://sharedspaces.intel.com/sites/PCDC/SitePages/Ingredients/ ingredient.aspx?ing=VT

Intel[®] Virtualization Technology (Intel[®] VT) for IA-32, Intel[®] 64 and Intel[®] Architecture (Intel[®] VT-X)

Intel[®] VT-x Objectives

Intel VT-x provides hardware acceleration for virtualization of IA platforms. Virtual Machine Monitor (VMM) can use Intel VT-x features to provide an improved reliable virtualized platform. By using Intel VT-x, a VMM is:

- Robust: VMMs no longer need to use para-virtualization or binary translation. This means that VMMs will be able to run off-the-shelf operating systems and applications without any special steps.
- **Enhanced:** Intel VT enables VMMs to run 64-bit guest operating systems on IA x86 processors.
- undefined undefined undefiner More reliable: Due to the hardware support, VMMs can now be smaller, less complex, and more efficient. This improves reliability and availability and reduces the potential for software conflicts.

3.1.1

- intel red under
 - More secure: The use of hardware transitions in the VMM strengthens the isolation of VMs and further prevents corruption of one VM from affecting others on the same system.

Intel[®] VT-x Key Features

The processor supports the following added new Intel VT-x features:

- Extended Page Table (EPT) Accessed and Dirty Bits
 - EPT A/D bits enabled VMMs to efficiently implement memory management and page classification algorithms to optimize VM memory operations, such as defragmentation, paging, live migration, and check-pointing. Without hardware support for EPT A/D bits, VMMs may need to emulate A/D bits by marking EPT paging-structures as not-present or read-only, and incur the overhead of EPT page-fault VM exits and associated software processing.
- EPTP (EPT pointer) switching
 - EPTP switching is a specific VM function. EPTP switching allows quest software (in VMX non-root operation, supported by EPT) to request a different EPT paging-structure hierarchy. This is a feature by which software in VMX non-root operation can request a change of EPTP without a VM exit. Software will be able to choose among a set of potential EPTP values determined in advance by software in VMX root operation.
- Pause loop exiting
 - Support VMM schedulers seeking to determine when a virtual processor of a multiprocessor virtual machine is not performing useful work. This situation may occur when not all virtual processors of the virtual machine are currently scheduled and when the virtual processor in question is in a loop involving the PAUSE instruction. The new feature allows detection of such loops and is thus called PAUSE-loop exiting.

undefined undefined unt The processor IA core supports the following Intel VT-x features:

- Mode based (XU/XS) EPT execute control New Feature for this processor
 - A new mode of EPT operation which enables different controls for executability of GPA based on Guest specified mode (User/Supervisor) of linear address translating to the GPA. When the mode is enabled, the executability of a GPA is defined by two bits in EPT entry. One bit for accesses to user pages and other one for accesses to supervisor pages.
 - The new mode requires changes in VMCS, and EPT entries. VMCS includes a bit "mode based EPT execute control" which is used to enable/disable the mode. An additional bit in EPT entry is defined as "supervisor-execute access"; the original execute control bit is considered as "user-execute access". If the "mode based EPT execute control" is disabled the additional bit is ignored and the system works with one bit execute control for both user pages and supervisor pages.
 - Behavioral changes Behavioral changes are across three areas:
 - Access to GPA- If the "mode-based EPT execute control" VM-execution control is 1, treatment of quest-physical accesses by instruction fetches depends on the linear address from which an instruction is being fetched
 - 1. If the translation of the linear address specifies user mode (the U/S bit was set in every paging structure entry used to translate the linear address), the resulting guest-physical address is executable under EPT only if the XU bit (at position 2) is set in every EPT pagingstructure entry used to translate the guest-physical address.
 - 2. If the translation of the linear address specifies supervisor mode (the U/S bit was clear in at least one of the paging-structure entries used

Datasheet, Volume 1 of 2 -4 undefined

Technologies .ogi uni ndefined undefined uni



to translate the linear address), the resulting guest-physical address is executable under EPT only if the XS bit is set in every EPT pagingstructure entry used to translate the quest-physical address

- -The XU and XS bits are used only when translating linear addresses for guest code fetches. They do not apply to guest page walks, data accesses, or A/D-bit updates
- VMEntry If the "activate secondary controls" and "mode-based EPT execute control" VM-execution controls are both 1, VM entries ensure that the "enable EPT" VM-execution control is 1. VM entry fails if this check fails. When such a failure occurs, control is passed to the next instruction,
- **VMExit** The exit qualification due to EPT violation reports clearly whether the violation was due to User mode access or supervisor mode access.
- ndefined undefined undefined Capability Querying: IA32 VMX PROCBASED CTLS2 has bit to indicate the capability, RDMSR can be used to read and query whether the processor supports the capability or not.
 - Extended Page Tables (EPT)
 - EPT is hardware assisted page table virtualization
 - It eliminates VM exits from quest OS to the VMM for shadow page-table maintenance
 - Virtual Processor IDs (VPID)
 - Ability to assign a VM ID to tag processor IA core hardware structures (such as TLBs)
 - This avoids flushes on VM transitions to give a lower-cost VM transition time and an overall reduction in virtualization overhead.
 - **Guest Preemption Timer**
 - Mechanism for a VMM to preempt the execution of a guest OS after an amount of time specified by the VMM. The VMM sets a timer value before entering a guest
 - The feature aids VMM developers in flexibility and Quality of Service (QoS) guarantees
 - Descriptor-Table Exiting
 - Descriptor-table exiting allows a VMM to protect a quest OS from internal (malicious software based) attack by preventing relocation of key system data structures like IDT (interrupt descriptor table), GDT (global descriptor table), LDT (local descriptor table), and TSS (task segment selector).
 - A VMM using this feature can intercept (by a VM exit) attempts to relocate these data structures and prevent them from being tampered by malicious software.

Intel[®] Virtualization Technology (Intel[®] VT) for Directed I/O (Intel[®] VT-d) 3.1.2

Intel[®] VT-d Objectives

The key Intel VT-d objectives are domain-based isolation and hardware-based virtualization. A domain can be abstractly defined as an isolated environment in a platform to which a subset of host physical memory is allocated. Intel VT-d provides accelerated I/O performance for a virtualized platform and provides software with the A undefined undefined undefined following capabilities:

• I/O device assignment and security: for flexibly assigning I/O devices to VMs and extending the protection and isolation properties of VMs for I/O operations.

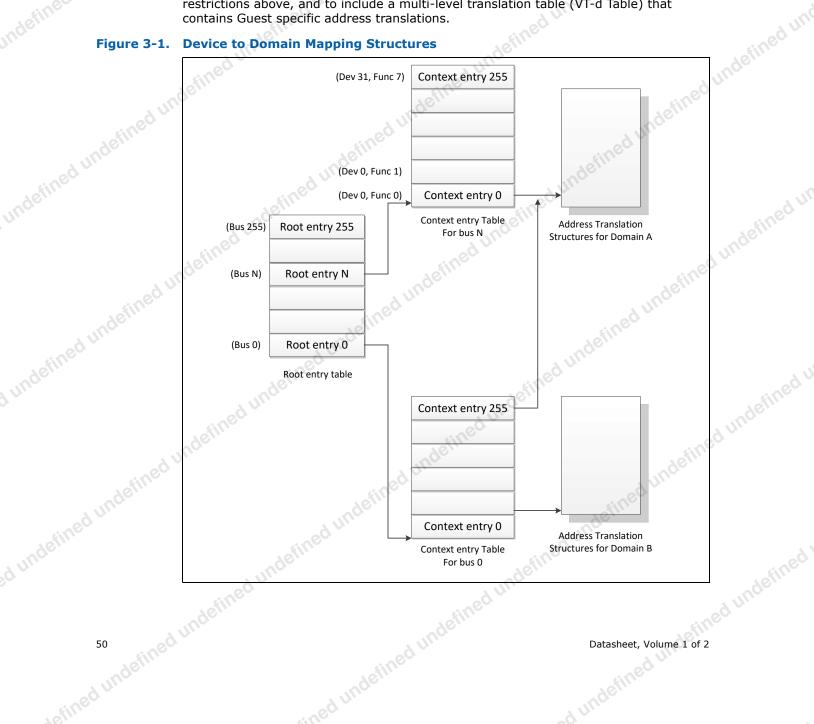
Datasheet, Volume 1 of 2 Infined Undel

(intel) red under

- DMA remapping: for supporting independent address translations for Direct Memory Accesses (DMA) from devices.
- Interrupt remapping: for supporting isolation and routing of interrupts from devices and external interrupt controllers to appropriate VMs.
- Reliability: for recording and reporting to system software DMA and interrupt errors that may otherwise corrupt memory or impact VM isolation.

Intel VT-d accomplishes address translation by associating transaction from a given I/O device to a translation table associated with the Guest to which the device is assigned. It does this by means of the data structure in the following illustration. This table creates an association between the device's PCI Express* Bus/Device/Function (B/D/F) number and the base address of a translation table. This data structure is populated by a VMM to map devices to translation tables in accordance with the device assignment restrictions above, and to include a multi-level translation table (VT-d Table) that contains Guest specific address translations.

Device to Domain Mapping Structures Figure 3-1.





ed undefined undefin Intel VT-d functionality, often referred to as an Intel VT-d Engine, has typically been implemented at or near a PCI Express* host bridge component of a computer system. This might be in a chipset component or in the PCI Express functionality of a processor with integrated I/O. When one such VT-d engine receives a PCI Express transaction from a PCI Express bus, it uses the B/D/F number associated with the transaction to search for an Intel VT-d translation table. In doing so, it uses the B/D/F number to traverse the data structure shown in the above figure. If it finds a valid Intel VT-d table in this data structure, it uses that table to translate the address provided on the PCI Express bus. If it does not find a valid translation table for a given translation, this results in an Intel VT-d fault. If Intel VT-d translation is required, the Intel VT-d engine performs an N-level table walk.

For more information, refer to Intel Virtualization Technology for Directed I/O Architecture Specification http://www.intel.com/content/dam/www/public/us/en/ documents/product-specifications/vt-directed-io-spec.pdf

Intel[®] VT-d Key Features

The processor supports the following Intel VT-d features:

- d undefined undefined un Memory controller and processor graphics comply with the Intel VT-d 2.1 Specification.
- Two Intel VT-d DMA remap engines.
 - iGFX DMA remap engine
 - Default DMA remap engine (covers all devices except iGFX)
- Support for root entry, context entry, and default context
- 39-bit guest physical address and host physical address widths
- Support for 4K page sizes only
- Support for register-based fault recording only (for single entry only) and support for MSI interrupts for faults
- Support for both leaf and non-leaf caching
- Support for boot protection of default page table
- Support for non-caching of invalid page table entries
- Support for hardware based flushing of translated but pending writes and pending reads, on IOTLB invalidation
- Support for Global, Domain specific and Page specific IOTLB invalidation
- MSI cycles (MemWr to address FEEx xxxxh) not translated
 - Translation faults result in cycle forwarding to VBIOS region (byte enables masked for writes). Returned data may be bogus for internal agents, PEG/DMI interfaces return unsupported request status
- Interrupt Remapping is supported
- Queued invalidation is supported
- Intel VT-d translation bypass address range is supported (Pass Through)

The processor supports the following added new Intel VT-d features:

A undefined undefined undefined 4-level Intel VT-d Page walk – both default Intel VT-d engine as well as the IGD VTd engine are upgraded to support 4-level Intel VT-d tables (adjusted guest address width of 48 bits) in the sundefined undefine



Indefined Technologies

• Intel VT-d superpage – support of Intel VT-d superpage (2 MB, 1 GB) for default Intel VT-d engine (that covers all devices except IGD) fined undefined un IGD Intel VT-d engine does not support superpage and BIOS should disable superpage in default Intel VT-d engine when iGfx is enabled.

Intel VT-d Technology may not be available on all SKUs.

Security Technologies 3.2

3.2.1

Note:

Intel[®] Trusted Execution Technology (Intel[®] TXT)

Intel[®] Trusted Execution Technology (Intel[®] TXT) defines platform-level enhancements that provide the building blocks for creating trusted platforms.

The Intel TXT platform helps to provide the authenticity of the controlling environment such that those wishing to rely on the platform can make an appropriate trust decision. The Intel TXT platform determines the identity of the controlling environment by accurately measuring and verifying the controlling software.

Another aspect of the trust decision is the ability of the platform to resist attempts to change the controlling environment. The Intel TXT platform will resist attempts by software processes to change the controlling environment or bypass the bounds set by the controlling environment.

Intel TXT is a set of extensions designed to provide a measured and controlled launch of system software that will then establish a protected environment for itself and any additional software that it may execute.

These extensions enhance two areas:

- The launching of the Measured Launched Environment (MLE).
- The protection of the MLE from potential corruption.

The enhanced platform provides these launch and control interfaces using Safer Mode Extensions (SMX).

The SMX interface includes the following functions:

- Measured/Verified launch of the MLE.
- Mechanisms to ensure the above measurement is protected and stored in a secure location.
- Protection mechanisms that allow the MLE to control attempts to modify itself.

The processor also offers additional enhancements to System Management Mode (SMM) architecture for enhanced security and performance. The processor provides new MSRs to:

- Enable a second SMM range
- Enable SMM code execution range checking
- Select whether SMM Save State is to be written to legacy SMRAM or to MSRs
- Determine if a thread is going to be delayed entering SMM.
- Determine if a thread is blocked from entering SMM
- Targeted SMI, enable/disable threads from responding to SMIs, both VLWs and IPI

Datasheet, Volume 1 of 2



d undefined undefin For the above features, BIOS should test the associated capability bit before attempting to access any of the above registers.

For more information, refer to the Intel® Trusted Execution Technology Measured Launched Environment Programming Guide

ndefined undefined Note:

3.2.2

Intel TXT Technology may not be available on all SKUs.

Intel[®] Advanced Encryption Standard New Instructions (Intel[®] AES-NI)

The processor supports Intel Advanced Encryption Standard New Instructions (Intel AES-NI) that are a set of Single Instruction Multiple Data (SIMD) instructions that enable fast and secure data encryption and decryption based on the Advanced Encryption Standard (AES). Intel AES-NI are valuable for a wide range of cryptographic applications, such as applications that perform bulk encryption/decryption, authentication, random number generation, and authenticated encryption. AES is broadly accepted as the standard for both government and industry applications, and is widely deployed in various protocols.

Intel AES-NI consists of six Intel SSE instructions. Four instructions, AESENC, AESENCLAST, AESDEC, and AESDELAST facilitate high performance AES encryption and decryption. The other two, AESIMC and AESKEYGENASSIST, support the AES key expansion procedure. Together, these instructions provide full hardware for supporting AES; offering security, high performance, and a great deal of flexibility.

undefined undefi Note:

3.2.3

Intel AES-NI Technology may not be available on all SKUs.

PCLMULQDQ (Perform Carry-Less Multiplication Quad word) Instruction

The processor supports the carry-less multiplication instruction, PCLMULODO. PCLMULQDQ is a Single Instruction Multiple Data (SIMD) instruction that computes the 128-bit carry-less multiplication of two 64-bit operands without generating and propagating carries. Carry-less multiplication is an essential processing component of several cryptographic systems and standards. Hence, accelerating carry-less multiplication can significantly contribute to achieving high speed secure computing and communication.

undefined undefinet Intel[®] Secure Key

The processor supports Intel Secure Key (formerly known as Digital Random Number Generator (DRNG)), a software visible random number generation mechanism supported by a high quality entropy source. This capability is available to programmers through the RDRAND instruction. The resultant random number generation capability is designed to comply with existing industry standards in this regard (ANSI X9.82 and NIST SP 800-90).

Some possible usages of the RDRAND instruction include cryptographic key generation as used in a variety of applications, including communication, digital signatures, secure undefined undefined undefined storage, and so on. A undefined undefined undefined

undefined undef Datasheet, Volume 1 of 2 Lotined undef

3.2.5

intel red unde

Execute Disable Bit The Execute Disable Bit allows memory to be marked as non executable when combined with a supporting operating system. If code attempts to run in nonundefined executable memory, the processor raises an error to the operating system. This feature can prevent some classes of viruses or worms that exploit buffer overrun vulnerabilities and can, thus, help improve the overall security of the system.

See the Intel 64 and IA-32 Architectures Software Developer's Manuals for more detailed information.

3.2.6 **Boot Guard Technology**

Boot Guard technology is a part of boot integrity protection technology. Boot Guard can help protect the platform boot integrity by preventing execution of unauthorized boot blocks. With Boot Guard, platform manufacturers can create boot policies such that invocation of an unauthorized (or untrusted) boot block will trigger the platform protection per the manufacturer's defined policy.

With verification based in the hardware, Boot Guard extends the trust boundary of the platform boot process down to the hardware level.

Boot Guard accomplishes this by:

- Providing of hardware-based Static Root of Trust for Measurement (S-RTM) and the Root of Trust for Verification (RTV) using Intel architectural components.
- Providing of architectural definition for platform manufacturer Boot Policy.
- Enforcing of manufacture provided Boot Policy using Intel architectural components.

Benefits of this protection is that Boot Guard can help maintain platform integrity by preventing re-purposing of the manufacturer's hardware to run an unauthorized software stack.

Intel[®] Supervisor Mode Execution Protection (SMEP)

Intel[®] Supervisor Mode Execution Protection (SMEP) is a mechanism that provides the next level of system protection by blocking malicious software attacks from user mode code when the system is running in the highest privilege level. This technology helps to protect from virus attacks and unwanted code from harming the system. For more information, refer to Intel[®] 64 and IA-32 Architectures Software Developer's Manual, Volume 3A at: http://www.intel.com/Assets/PDF/manual/253668.pdf

Intel[®] Supervisor Mode Access Protection (SMAP) 3.2.8

Intel[®] Supervisor Mode Access Protection (SMAP) is a mechanism that provides next level of system protection by blocking a malicious user from tricking the operating system into branching off user data. This technology shuts down very popular attack vectors against operating systems.

For more information, refer to the Intel [®] 64 and IA-32 Architectures Software Developer's Manual, Volume 3A: http://www.intel.com/Assets/PDF/manual/253668.pdf

> Datasheet, Volume 1 of 2 -4 undefined





Intel[®] Memory Protection Extensions (Intel[®] MPX) 3.2.9

Intel[®] MPX provides hardware accelerated mechanism for memory testing (heap and stack) buffer boundaries in order to identify buffer overflow attacks.

An Intel MPX enabled compiler inserts new instructions that tests memory boundaries prior to a buffer access. Other Intel MPX commands are used to modify a database of memory regions used by the boundary checker instructions.

The Intel MPX ISA is designed for backward compatibility and will be treated as nooperation instructions (NOPs) on older processors.

Intel MPX can be used for:

- · Efficient runtime memory boundary checks for security-sensitive portions of the application.
- As part of a memory checker tool for finding difficult memory access errors. Intel MPX is significantly of magnitude faster than software implementations.

Intel MPX emulation (without hardware acceleration) is available with the Intel C++ Compiler 13.0 or newer.

For more information, refer to the Intel MPX documentation.

undefined und 3.2.10

Intel[®] Software Guard Extensions (Intel[®] SGX)

Software Guard Extensions (SGX) is a processor enhancement designed to help protect application integrity and confidentiality of secrets and withstands software and certain hardware attacks.

Software Guard Extensions (SGX) creates and operates in protected regions of memory named Enclaves.

Enclave code can be accessed using new special ISA commands that jump into per Enclave predefined addresses. Data within an Enclave can only be accessed from that same Enclave code.

The latter security statements hold under all privilege levels including supervisor mode (ring-0), System Management Mode (SMM) and other Enclaves.

Software Guard Extensions (SGX) features a memory encryption engine that both ined undefined encrypt Enclave memory as well as protect it from corruption and replay attacks.

Software Guard Extensions (SGX) benefits over alternative Trusted Execution Environments (TEEs) are:

- Enclaves are written using C/C++ using industry standard build tools.
- High processing power as they run on the processor.
- Large amount of memory are available as well as non-volatile storage (such as disk drives).
- Simple to maintain and debug using standard IDEs (Integrated Development A undefined undefined undefined Environment)
- Scalable to a larger number of applications and vendors running concurrently

For more information, refer to the Intel[®] SGX Website.

Datasheet, Volume 1 of 2 Intined Undel



Intel[®] Virtualization Technology (Intel[®] VT) for Directed I/O (Intel[®] VT-d) 3.2.11

undefined un Refer to Section 3.1.2, "Intel[®] Virtualization Technology (Intel[®] VT) for Directed I/O (Intel[®] VT-d)" Intel VT-d for detail.

Power and Performance Technologies 3.3

Intel[®] Hyper-Threading Technology (Intel[®] HT Technology)

The processor supports Intel[®] Hyper-Threading Technology (Intel[®] HT Technology) that allows an execution processor IA core to function as two logical processors. While some execution resources such as caches, execution units, and buses are shared, each ined undefined logical processor has its own architectural state with its own set of general-purpose registers and control registers. This feature should be enabled using the BIOS and requires operating system support.

Note:

Intel HT Technology may not be available on all SKUs.

Intel[®] Turbo Boost Technology 2.0

The Intel[®] Turbo Boost Technology 2.0 allows the processor IA core / processor graphics core to opportunistically and automatically run faster than the processor IA core base frequency / processor graphics base frequency if it is operating below power, temperature, and current limits. The Intel Turbo Boost Technology 2.0 feature is designed to increase performance of both multi-threaded and single-threaded workloads.

Compared with previous generation products, Intel Turbo Boost Technology 2.0 will increase the ratio of application power towards TDP and also allows to increase power above TDP as high as PL2 for short periods of time. Thus, thermal solutions and platform cooling that are designed to less than thermal design guidance might experience thermal and performance issues since more applications will tend to run at the maximum power limit for significant periods of time.

Note:

Intel Turbo Boost Technology 2.0 may not be available on all SKUs.

Intel[®] Turbo Boost Technology 2.0 Frequency 3.3.2.1

To determine the highest performance frequency amongst active processor IA cores, the processor takes the following into consideration:

- The number of processor IA cores operating in the C0 state.
- The estimated processor IA core current consumption and I_{CCMax} register settings.
- The estimated package prior and present power consumption and turbo power limits.
- The package temperature.
- Sustained turbo residencies at high voltages and temperature. in a sum defined undefined unde

Datasheet, Volume 1 of 2 . . undefined



ad undefined undefine Any of these factors can affect the maximum frequency for a given workload. If the power, current, Voltage or thermal limit is reached, the processor will automatically reduce the frequency to stay within the PL1 value. Turbo processor frequencies are only undefined un active if the operating system is requesting the P0 state. If turbo frequencies are limited the cause is logged in IA PERF LIMIT REASONS register. For more information on P-states and C-states, see Chapter 4, "Power Management".

Intel[®] Advanced Vector Extensions 2 (Intel[®] AVX2) 3.3.3

Intel[®] Advanced Vector Extensions 2.0 (Intel[®] AVX2) is the latest expansion of the Intel instruction set. Intel AVX2 extends the Intel Advanced Vector Extensions (Intel AVX) with 256-bit integer instructions, floating-point fused multiply add (FMA) instructions, and gather operations. The 256-bit integer vectors benefit math, codec, image, and digital signal processing software. FMA improves performance in face detection, professional imaging, and high performance computing. Gather operations increase vectorization opportunities for many applications. In addition to the vector extensions, this generation of Intel processors adds new bit manipulation instructions useful in compression, encryption, and general purpose software. For more information on Intel AVX, see http://www.intel.com/software/avx

Intel Advanced Vector Extensions (Intel AVX) are designed to achieve higher throughput to certain integer and floating point operation. Due to varying processor power characteristics, utilizing AVX instructions may cause a) parts to operate below the base frequency b) some parts with Intel Turbo Boost Technology 2.0 to not achieve any or maximum turbo frequencies. Performance varies depending on hardware, software and system configuration and you should consult your system manufacturer for more information. Intel Advanced Vector Extensions refers to Intel AVX, Intel AVX2 or Intel AVX-512.

stined undefined For more information on Intel AVX, see http://www-ssl.intel.com/content/www/us/en/ architecture-and-technology/turbo-boost/turbo-boost-technology.html

Note:

Intel AVX2 Technology may not be available on all SKUs.

Intel[®] 64 Architecture x2APIC

The x2APIC architecture extends the xAPIC architecture that provides key mechanisms for interrupt delivery. This extension is primarily intended to increase processor addressability.

Specifically, x2APIC:

- Retains all key elements of compatibility to the xAPIC architecture:
 - Delivery modes
 - Interrupt and processor priorities
 - Interrupt sources
 - Interrupt destination types
- Provides extensions to scale processor addressability for both the logical and physical destination modes
- Adds new features to enhance performance of interrupt delivery
- A undefined undefined undefined Reduces complexity of logical destination mode interrupt delivery on link based in a undefined undefined un architectures

The key enhancements provided by the x2APIC architecture over xAPIC are the following:

- Support for two modes of operation to provide backward compatibility and extensibility for future platform innovations:
 - In xAPIC compatibility mode, APIC registers are accessed through memory mapped interface to a 4K-Byte page, identical to the xAPIC architecture.
 - In x2APIC mode, APIC registers are accessed through Model Specific Register (MSR) interfaces. In this mode, the x2APIC architecture provides significantly increased processor addressability and some enhancements on interrupt delivery.
- Increased range of processor addressability in x2APIC mode:
 - Physical xAPIC ID field increases from 8 bits to 32 bits, allowing for interrupt processor addressability up to 4G-1 processors in physical destination mode. A processor implementation of x2APIC architecture can support fewer than 32bits in a software transparent fashion.
 - Logical xAPIC ID field increases from 8 bits to 32 bits. The 32-bit logical x2APIC ID is partitioned into two sub-fields – a 16-bit cluster ID and a 16-bit logical ID within the cluster. Consequently, $((2^20) - 16)$ processors can be addressed in logical destination mode. Processor implementations can support fewer than 16 bits in the cluster ID sub-field and logical ID sub-field in a software agnostic fashion.
- More efficient MSR interface to access APIC registers:
 - To enhance inter-processor and self-directed interrupt delivery as well as the ability to virtualize the local APIC, the APIC register set can be accessed only through MSR-based interfaces in x2APIC mode. The Memory Mapped IO (MMIO) interface used by xAPIC is not supported in x2APIC mode.
- undefined undefined unde The semantics for accessing APIC registers have been revised to simplify the programming of frequently-used APIC registers by system software. Specifically, the software semantics for using the Interrupt Command Register (ICR) and End Of Interrupt (EOI) registers have been modified to allow for more efficient delivery and dispatching of interrupts.
 - The x2APIC extensions are made available to system software by enabling the local x2APIC unit in the "x2APIC" mode. To benefit from x2APIC capabilities, a new operating system and a new BIOS are both needed, with special support for x2APIC mode.
 - The x2APIC architecture provides backward compatibility to the xAPIC architecture and forward extendible for future Intel platform innovations. ined undefined

Note:

intel red under

Intel x2APIC Technology may not be available on all SKUs.

For more information, see the Intel[®] 64 Architecture x2APIC Specification at http:// www.intel.com/products/processor/manuals/.

Power Aware Interrupt Routing (PAIR)

The processor includes enhanced power-performance technology that routes interrupts to threads or processor IA cores based on their sleep states. As an example, for energy savings, it routes the interrupt to the active processor IA cores without waking the deep idle processor IA cores. For performance, it routes the interrupt to the idle (C1) processor IA cores without interrupting the already heavily loaded processor IA cores. This enhancement is mostly beneficial for high-interrupt scenarios like Gigabit LAN, WLAN peripherals, and so on. weinen undefined unde

Datasheet, Volume 1 of 2 -4 undefined

Technologies



3.3.6

3.4

Intel[®] Transactional Synchronization Extensions (Intel[®] TSX-NI)

Intel[®] Transactional Synchronization Extensions (Intel[®] TSX-NI) provides a set of instruction set extensions that allow programmers to specify regions of code for transactional synchronization. Programmers can use these extensions to achieve the performance of fine-grain locking while actually programming using coarse-grain locks. Details on Intel TSX-NI may be found in Intel[®] Architecture Instruction Set Extensions Programming Reference. Intel TSX-NI may not be available on all SKUs. Intel® Image Signal Processor (Intel[®] ISP)

Platform Imaging Infrastructure

Note:

Intel TSX-NI may not be available on all SKUs.

The imaging infrastructure is based on a number of hardware components as shown in Figure 3-3, "Platform Imaging Infrastructure". The three major components of the system are:

- Camera SubSystem: Located in the lid of the system and contains CMOS sensor, flash, LED, I/O interface (MIPI* CSI-2 and I²C*), Focus control and other components.
- **Camera I/O controller:** The I/O controller is located in the PCH and contains a MIPI-CSI2 Host controller. The host controller is a PCI device (independent of the ISP device). The CSI-2 HCI brings imaging data from an external imager into the system and provides a command and control channel for the imager using I^2C .

Datasheet, Volume 1 of 2 wined undef



Technologies

Figure 3-2. Processor Camera System

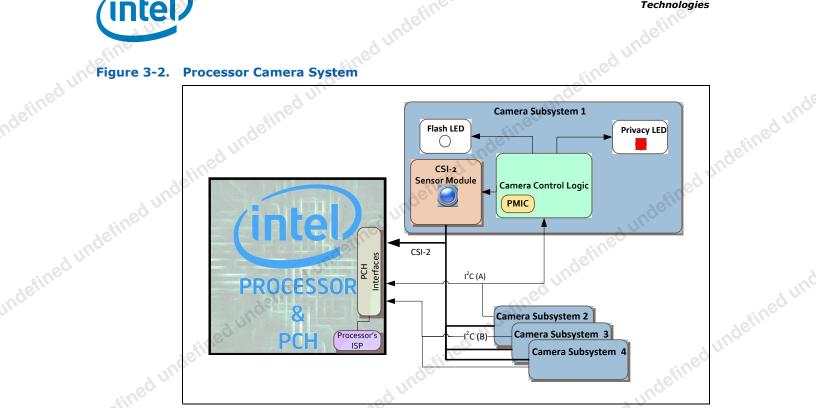
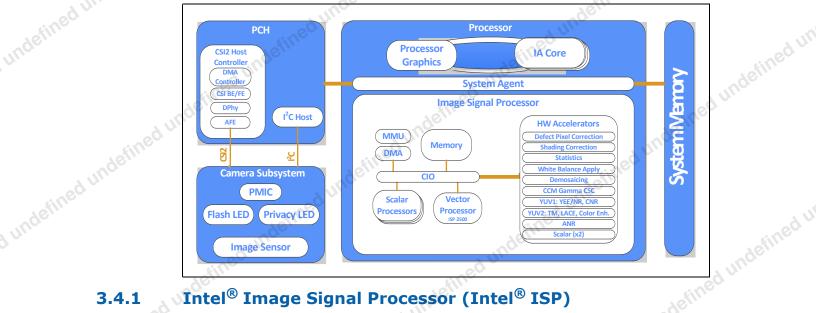


Figure 3-3.

Platform Imaging Infrastructure



3.4.1

3.5

Intel[®] Image Signal Processor (Intel[®] ISP)

The Intel ISP is an embedded camera subsystem hardware component on the processor, it processes video and still images at high quality with a low-power cost by leveraging a programmable VLIW (very-long-instruction-word) SIMD vector processor, a hardware fixed function pipe (accelerators), two scalar processor, and more. The mix of hardware accelerators and compute capabilities allows the flexibility and patchability that are required for late changes and allowing the unit to support future sensor ace undefined undefined g undefined undefin

Datasheet, Volume 1 of 2 -4 undefined

d undefined



ned undefined underined technologies while remaining in an optimized power performance point. Debug Technologies

ndefined undefined 3.5.1

Intel[®] Processor Trace (Intel[®] PT) is a new tracing capability added to Intel Architecture, for use in software debug and profiling. Intel PT provides the capability for more precise software control flow and timing information, with limited impact to software execution. This provides enhanced ability to debug software or other anomalies, as well as responsiveness

a underned Intel VTune[™] Amplifier for Systems and the Intel System Debugger are part of Intel System Studio 2015, which includes updates for new debug and trace features on this

Power Management undermed und

(intel) and underine

ndefined und

4

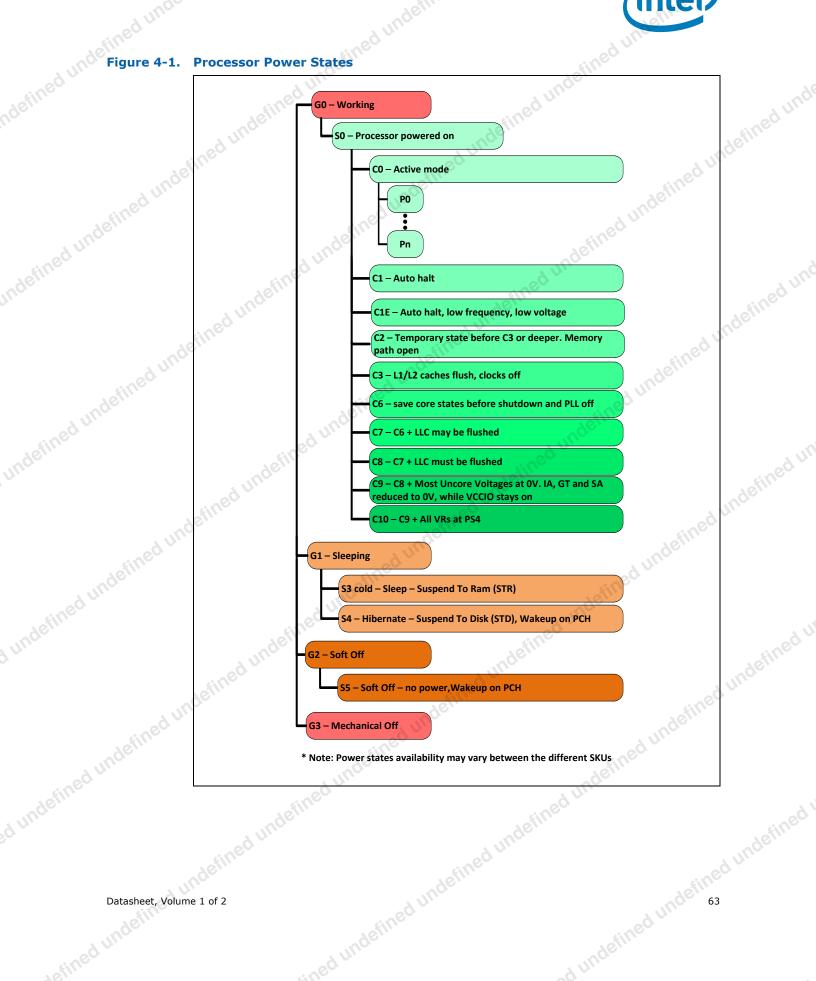
- Jundermed undermed undermed

2 Mark making making water and under med under med



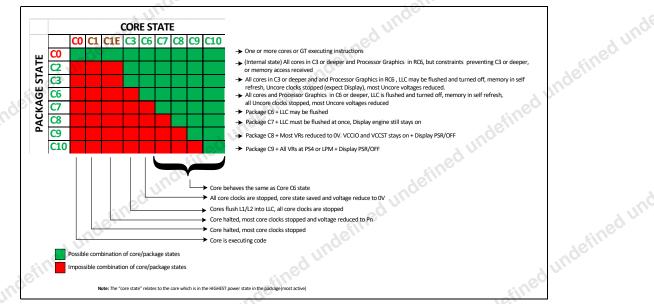
Processor Power States Figure 4-1.

Jed undernie





led undefined undefined Figure 4-2. Processor Package and IA Core C-States



Note: 00 undefined unde

If the Platform does not support Modern Standby (Previously known as Connected Standby) and does not support PS4, it is recommended to limit the package state to package C9 (Better power).

Table 4-1. **System States** undefined undefined

			un de.	
undefined	4.1	Advanc (ACPI)	ed Configuration and Power Interface States Supported	d undefined u
•		This section	describes the ACPI states supported by the processor.	
	Table 4-1.	System Sta	tes stine ⁰	ed un.
	-du	State	Description	
		G0/S0	Full On	
undefined	unde	G1/S3-Cold	Suspend-to-RAM (STR). Context saved to memory (S3-Hot is not supported by the processor).	
		G1/S4	Suspend-to-Disk (STD). All power lost (except wake-up on PCH).	
der		G2/S5	Soft off. All power lost (except wake-up on PCH). Total reboot.	undefined '
J UN		G3	Mechanical off. All power removed from system.	sines
ad undefine	d undefined	- 6	Datasheet, Volume 1	defined
a fin	64 ad undefined	undefinec	Datasheet, Volume 1	ined unc. of 2



Red undefined undefined ndefined undefined Processor IA Core / Package State Support Table 4-2.

	State	Description	_
	C0	Active mode, processor executing code.	
	C1	AutoHALT processor IA core state (package C0 state).	sineu
	C1E	AutoHALT processor IA core state with lowest frequency and voltage operating point (package C0 state).	dell
unde	C2	All processor IA cores in C3 or deeper. Memory path open. Temporary state before Package C3 or deeper.	
	C3	Processor IA execution cores in C3 or deeper, flush their L1 instruction cache, L1 data cache, and L2 cache to the LLC shared cache. LLC may be flushed. Clocks are shut off to each core.	
under.	C6	Processor IA execution cores in this state save their architectural state before removing core voltage. BCLK is off.	
efined	C7	Processor IA execution cores in this state behave similarly to the C6 state. If all execution cores request C7, LLC ways may be flushed until it is cleared. If the entire LLC is flushed, voltage will be removed from the LLC.	20
	C8	C7 plus LLC should be flushed.	sinec
	C9	C8 plus most Uncore voltages at 0V. IA, GT and SA reduced to 0V, while Vcc_{IO} stays on.	der.
× C	C10	C9 plus all VRs at PS4 or LPM. 24 MHz clock off	
Table 4-3.	Integrated N	Iemory Controller (IMC) States	
efines	State	Description	

Table 4-3. Integrated Memory Controller (IMC) States

State	Description
Power up	CKE asserted. Active mode.
Pre-charge Power down	CKE de-asserted (not self-refresh) with all banks closed.
Active Power down	CKE de-asserted (not self-refresh) with minimum one bank active.
Self-Refresh	CKE de-asserted using device self-refresh.

Table 4-4. **PCI Express* Link States**

PCI Expres	s* Link States	2
State	Description	18fineu
LO	Full on – Active transfer state.	4 UNO
L1	Lowest Active Power Management – Longer exit latency	cinec
L3	Lowest power state (power-off) – Longest exit latency	dein

undefined undefined Table 4-5.

Direct Media Interface (DMI) States

eQ.	L3	Lowest power state (power-off) – Longest exit latency	
Table 4-5.	Direct Media	Interface (DMI) States	
d une	State	Description	ofineu
	LO	Full on – Active transfer state	inde
	L1	Lowest Active Power Management – Longer exit latency	ed U
	L3	Lowest power state (power-off) – Longest exit latency	efille
in ^{eo}		du.	
defin			
d undefined undefined un		defined undefined	
sineu		dui uno	
dell		atine	21
d ulli		de	aned undefined i
20.	ed v.	, unc	dein
	stine		d un
	nois	deth	stines
Datasheet, Volum	ne 1 of 2	A UNC	65
18/111		defined unoe	
unoc		den	
med undefin		defined undefined un	
18111		aner dur	



Table 4-6.

led undefined undefine G, S, and C Interface State Combinations

(Intel)			etine			Power Management	
		d C Interfac	e State Combir	ations		ned undefil.	
defined une table 4-0.	Global (G) State	Sleep (S) State	Processor Package (C) State	Processor State	System Clocks	Description	
	G0	S0	C0	Full On	On	Full On	
	G0	S0	C1/C1E	Auto-Halt	On	Auto-Halt	
54	G0	S0	C3	Deep Sleep	On	Deep Sleep	
defined undefined und	G0	S0	C6/C7	Deep Power Down	On	Deep Power Down	
stines	G0	S0	C8/C9/C10	Off	On	Deeper Power Down	
nder	G1	S3	Power off	Off	Off, except RTC	Suspend to RAM	
dui	G1	S4	Power off	Off	Off, except RTC	Suspend to Disk	
fine	G2	S5	Power off	Off	Off, except RTC	Soft Off	
70.	G3	N/A	Power off	Off	Power off	Hard off	

4.2

Processor IA Core Power Management

While executing code, Enhanced Intel SpeedStep Technology and Intel Speed Shift[®] Technology optimizes the processor's IA core frequency and voltage based on workload. Each frequency and voltage operating point is defined by ACPI as a P-state. When the processor is not executing code, it is idle. A low-power idle state is defined by ACPI as a C-state. In general, deeper power C-states have longer entry and exit latencies.

undefined undefit **OS/HW controlled P-states** 4.2.1

Enhanced Intel[®] SpeedStep[®] Technology 4.2.1.1

Enhanced Intel[®] SpeedStep[®] Technology enables OS to control and select P-state. The following are the key features of Enhanced Intel SpeedStep Technology:

- Multiple frequency and voltage points for optimal performance and power efficiency. These operating points are known as P-states.
- Frequency selection is software controlled by writing to processor MSRs. The voltage is optimized based on the selected frequency and the number of active processor IA cores.
 - Once the voltage is established, the PLL locks on to the target frequency.
 - All active processor IA cores share the same frequency and voltage. In a multicore processor, the highest frequency P-state requested among all active IA cores is selected.
 - Software-requested transitions are accepted at any time. If a previous transition is in progress, the new transition is deferred until the previous transition is completed.
- The processor controls voltage ramp rates internally to ensure glitch-free transitions.
- Because there is low transition latency between P-states, a significant number of undefined undefined undefined transitions per-second are possible.

ined undef

Caution:



4.2.1.2 Intel[®] Speed Shift Technology

Intel Speed Shift Technology is an energy efficient method of frequency control by the hardware rather than relying on OS control. OS is aware of available hardware P-states and request a desired P-state or it can let Hardware determine the P-state. The OS request is based on its workload requirements and awareness of processor capabilities. Processor decision is based on the different system constraints for example: Workload demand, thermal limits while taking into consideration the minimum and maximum levels and activity window of performance requested by the operating system.

For more details, refer to the following document (see related documents section):

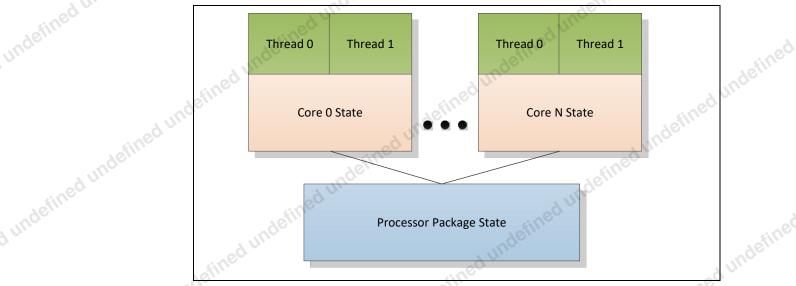
• Intel[®] 64 and IA-32 Architectures Software Developer's Manual (SDM), volume 3B.

4.2.2 Low-Power Idle States

When the processor is idle, low-power idle states (C-states) are used to save power. More power savings actions are taken for numerically higher C-states. However, deeper C-states have longer exit and entry latencies. Resolution of C-states occur at the thread, processor IA core, and processor package level. Thread-level C-states are available if Intel Hyper-Threading Technology is enabled.

Long term reliability cannot be assured unless all the Low-Power Idle States are enabled.

Figure 4-3. Idle Power Management Breakdown of the Processor IA Cores



While individual threads can request low-power C-states, power saving actions only take place once the processor IA core C-state is resolved. processor IA core C-states are automatically resolved by the processor. For thread and processor IA core C-states, a transition to and from C0 state is required before entering any other C-state.

Datasheet, Volume 1 of 2

intel ned under

Requesting Low-Power Idle States

The primary software interfaces for requesting low-power idle states are through the MWAIT instruction with sub-state hints and the HLT instruction (for C1 and C1E). However, software may make C-state requests using the legacy method of I/O reads from the ACPI-defined processor clock control registers, referred to as P_LVLx. This method of requesting C-states provides legacy support for operating systems that initiate C-state transitions using I/O reads.

For legacy operating systems, P LVLx I/O reads are converted within the processor to the equivalent MWAIT C-state request. Therefore, P_LVLx reads do not directly result in I/O reads to the system. The feature, known as I/O MWAIT redirection, should be enabled in the BIOS.

The BIOS can write to the C-state range field of the PMG IO CAPTURE MSR to restrict the range of I/O addresses that are trapped and emulate MWAIT like functionality. Any P LVLx reads outside of this range do not cause an I/O redirection to MWAIT(Cx) like request. They fall through like a normal I/O instruction.

When P LVLx I/O instructions are used, MWAIT sub-states cannot be defined. The MWAIT sub-state is always zero if I/O MWAIT redirection is used. By default, P_LVLx I/O redirections enable the MWAIT 'break on EFLAGS.IF' feature that triggers a wake up on an interrupt, even if interrupts are masked by EFLAGS.IF.

Processor IA Core C-State Rules

The following are general rules for all processor IA core C-states, unless specified otherwise:

- A processor IA core C-State is determined by the lowest numerical thread state (such as Thread 0 requests C1E while Thread 1 requests C3 state, resulting in a processor IA core C1E state). See the G, S, and C Interface State Combinations table.
- A processor IA core transitions to C0 state when:
 - An interrupt occurs
 - There is an access to the monitored address if the state was entered using an MWAIT/Timed MWAIT instruction
 - The deadline corresponding to the Timed MWAIT instruction expires
- An interrupt directed toward a single thread wakes up only that thread.
- If any thread in a processor IA core is active (in C0 state), the core's C-state will resolve to C0.
- Any interrupt coming into the processor package may wake any processor IA core
- A system reset re-initializes all processor IA cores.

processor IA core C0 State

The normal operating state of a processor IA core where code is being executed.

processor IA core C1/C1E State

C1/C1E is a low-power state entered when all threads within a processor IA core execute a HLT or MWAIT(C1/C1E) instruction. immed undefined undefined

Datasheet, Volume 1 of 2 . A undefined

ur4.5



A System Management Interrupt (SMI) handler returns execution to either Normal state or the C1/C1E state. See the Intel 64 and IA-32 Architectures Software Developer's Manual for more information.

While a processor IA core is in C1/C1E state, it processes bus snoops and snoops from other threads. For more information on C1E, see Section 4.2.5, "Package C-States".

processor IA core C3 State

Individual threads of a processor IA core can enter the C3 state by initiating a P LVL2 I/O read to the P BLK or an MWAIT(C3) instruction. A processor IA core in C3 state flushes the contents of its L1 instruction cache, L1 data cache, and L2 cache to the shared LLC, while maintaining its architectural state. All processor IA core clocks are stopped at this point. Because the processor IA core's caches are flushed, the processor does not wake any processor IA core that is in the C3 state when either a snoop is detected or when another processor IA core accesses cacheable memory.

processor IA core C6 State

Individual threads of a processor IA core can enter the C6 state by initiating a P_LVL3 I/O read or an MWAIT(C6) instruction. Before entering processor IA core C6 state, the processor IA core will save its architectural state to a dedicated SRAM. Once complete, a processor IA core will have its voltage reduced to zero volts. During exit, the processor IA core is powered on and its architectural state is restored.

processor IA core C7-C10 States

Individual threads of a processor IA core can enter the C7, C8, C9, or C10 state by initiating a P_LVL4, P_LVL5, P_LVL6, P_LVL7 I/O read (respectively) to the P_BLK or by undefiner an MWAIT(C7/C8/C9/C10) instruction. The processor IA core C7-C10 state exhibits the same behavior as the processor IA core C6 state.

C-State Auto-Demotion

In general, deeper C-states, such as C6 or C7, have long latencies and have higher energy entry/exit costs. The resulting performance and energy penalties become significant when the entry/exit frequency of a deeper C-state is high. Therefore, incorrect or inefficient usage of deeper C-states have a negative impact on battery life and idle power. To increase residency and improve battery life and idle power in deeper C-states, the processor supports C-state auto-demotion.

There are two C-State auto-demotion options:

- C7/C6 to C3
- C7/C6/C3 To C1

The decision to demote a processor IA core from C6/C7 to C3 or C3/C6/C7 to C1 is based on each processor IA core's immediate residency history. Upon each processor IA core C6/C7 request, the processor IA core C-state is demoted to C3 or C1 until a sufficient amount of residency has been established. At that point, a processor IA core is allowed to go into C3/C6 or C7. Each option can be run concurrently or individually. If the interrupt rate experienced on a processor IA core is high and the processor IA core A undefined undefined undefined is rarely in a deep C-state between such interrupts, the processor IA core can be demoted to a C3 or C1 state. A higher interrupt pattern is required to demote a processor IA core to C1 as compared to C3. it and undefined undefined ut

Datasheet, Volume 1 of 2 weined under



ad undefined undefined This feature is disabled by default. BIOS should enable it in the PMG_CST_CONFIG_CONTROL register. The auto-demotion policy is also configured by this register.

4.2.5 **Package C-States**

The processor supports C0, C2, C3, C6, C7, C8, C9, and C10 package states. The following is a summary of the general rules for package C-state entry. These apply to all package C-states, unless specified otherwise:

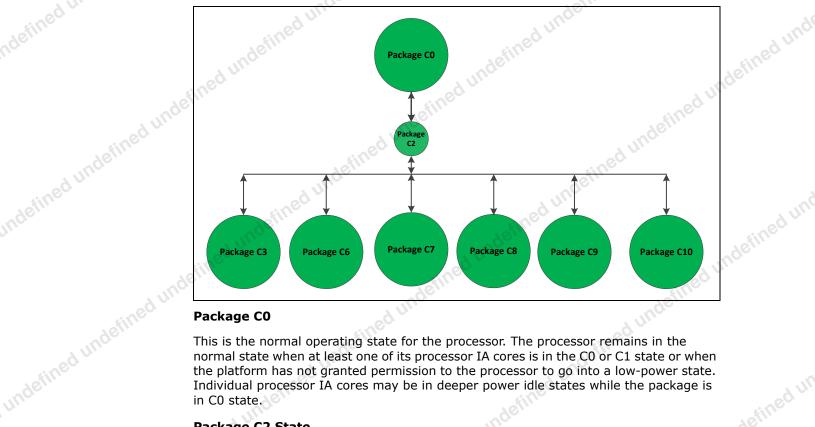
- A package C-state request is determined by the lowest numerical processor IA core C-state amongst all processor IA cores.
- A package C-state is automatically resolved by the processor depending on the processor IA core idle power states and the status of the platform components.
 - Each processor IA core can be at a lower idle power state than the package if the platform does not grant the processor permission to enter a requested package C-state.
 - The platform may allow additional power savings to be realized in the processor.
 - For package C-states, the processor is not required to enter C0 before entering any other C-state.
 - Entry into a package C-state may be subject to auto-demotion that is, the processor may keep the package in a deeper package C-state then requested by the operating system if the processor determines, using heuristics, that the deeper C-state results in better power/performance.

undefined undefined und The processor exits a package C-state when a break event is detected. Depending on the type of break event, the processor does the following:

- If a processor IA core break event is received, the target processor IA core is activated and the break event message is forwarded to the target processor IA core.
 - If the break event is not masked, the target processor IA core enters the processor IA core C0 state and the processor enters package C0.
 - If the break event is masked, the processor attempts to re-enter its previous package state.
- If the break event was due to a memory access or snoop request,
- " undefined unde But the platform did not request to keep the processor in a higher package Cstate, the package returns to its previous C-state.
- And the platform requests a higher power C-state, the memory access or snoop d undefined undefined undefi request is serviced and the package remains in the higher power C-state.



Figure 4-4. Package C-State Entry and Exit



Package C0

This is the normal operating state for the processor. The processor remains in the normal state when at least one of its processor IA cores is in the C0 or C1 state or when the platform has not granted permission to the processor to go into a low-power state. Individual processor IA cores may be in deeper power idle states while the package is in C0 state.

Package C2 State

Package C2 state is an internal processor state that cannot be explicitly requested by software. A processor enters Package C2 state when either:

- All processor IA cores have requested a C3 or deeper power state and all graphics processor IA cores requested are in RC6, but constraints (LTR, programmed timer events in the near future, and so forth) prevent entry to any state deeper than C2 state.
- undefined undefined • Or, all processor IA cores have requested a C3 or deeper power state and all graphics processor IA cores requested are in RC6 and a memory access request is received. Upon completion of all outstanding memory requests, the processor transitions back into a deeper package C-state.

Package C3 State

A processor enters the package C3 low-power state when:

- At least one processor IA core is in the C3 state.
- The other processor IA cores are in a C3 or deeper power state, and the processor ٠ has been granted permission by the platform.
- A undefined undefined undefined The platform has not granted a request to a package C6/C7 state or deeper state but has allowed a package C3 state.

In package C3-state, the LLC shared cache is valid. in a undefined undefin

Datasheet, Volume 1 of 2 weined undef

Package C6 State

intel red unde

A processor enters the package C6 low-power state when:

- At least one processor IA core is in the C6 state.
- The other processor IA cores are in a C6 or deeper power state, and the processor has been granted permission by the platform.
- The platform has not granted a package C7 or deeper request but has allowed a C6 package state.

In package C6 state, all processor IA cores have saved their architectural state and have had their voltages reduced to zero volts. It is possible the LLC shared cache is flushed and turned off in package C6 state.

Package C7 State

The processor enters the package C7 low-power state when all processor IA cores are in the C7 or deeper state and the operating system may request that the LLC will be flushed.

processor IA core break events are handled the same way as in package C3 or C6.

Upon exit of the package C7 state, the LLC will be partially enabled once a processor IA core wakes up if it was fully flushed, and will be fully enabled once the processor has stayed out of C7 for a preset amount of time. Power is saved since this prevents the LLC from being re-populated only to be immediately flushed again. Some VRs are reduce to 0V.

Package C8 State

The processor enters C8 states when the processor IA cores lower numerical state is C8.

The C8 state is similar to C7 state, but in addition, the LLC is flushed in a single step, Vcc and Vcc_{GT} are reduced to 0V. The display engine stays on.

Package C9 State

The processor enters C9 states when the processor IA cores lower numerical state is C9.

Package C9 state is similar to C8 state; the VRs are off, Vcc, Vcc_{GT} and Vcc_{SA} at 0V, Vcc_{IO} and Vcc_{ST} stays on.

Package C10 State

The processor enters C10 states when the processor IA cores lower numerical state is C10.

Package C10 state is similar to the package C9 state, but in addition the IMVP8 VR is in PS4 low-power state, which is near to shut off of the IMVP8 VR. The Vcc_{IO} is in low-power mode as well.

Datasheet, Volume 1 of 2



InstantGo

Jefined undefined undefi InstantGo is a platform state. On display time out the OS requests the processor to enter package C10 and platform devices at RTD3 (or disabled) in order to attain low power in idle.

Dynamic LLC Sizing

When all processor IA cores request C7 or deeper C-state, internal heuristics dynamically flushes the LLC. Once the processor IA cores enter a deep C-state, depending on their MWAIT sub-state request, the LLC is either gradually flushed Nways at a time or flushed all at once. Upon the processor IA cores exiting to C0 state, the LLC is gradually expanded based on internal heuristics.

fined undef 4.2.6

undefined undefin

Package C-States and Display Resolutions

The integrated graphics engine has the frame buffer located in system memory. When the display is updated, the graphics engine fetches display data from system memory. Different screen resolutions and refresh rates have different memory latency requirements. These requirements may limit the deepest Package C-state the processor can enter. Other elements that may affect the deepest Package C-state available are the following:

- · Display is on or off
- Single or multiple displays
- Native or non-native resolution
- Panel Self Refresh (PSR) technology

Display resolution is not the only factor influencing the deepest Package C-state the processor can get into. Device latencies, interrupt response latencies, and core C-states are among other factors that influence the final package C-state the processor can enter.

The following table lists display resolutions and deepest available package C-State.The display resolutions are examples using common values for blanking and pixel rate. Actual results will vary. The table shows the deepest possible Package C-state.System workload, system idle, and AC or DC power also affect the deepest possible Package Cstate.

Table 4-7.

undefined undefined un

Note:

Deepest Package C-State Available (Sheet 1 of 2)

. unc.		, uno-	Y/U Proces	ssor Line ^{1,2}
Resolution	Number of Displays	Resolution	PSR Enabled	e (Sheet ssor Line ^{1,2} PSR Disabled PC8 PC8 PC8 PC8 PC8 PC8 PC8 PC8 PC8 PC8
800x600 60Hz	Single	0x600 60Hz	PC10	PC8
1024x768 60Hz	Single	24x768 60Hz	PC10	PC8
1280x1024 60Hz	Single	80x1024 60Hz	PC10	PC8
1920x1080 60Hz	Single	20x1080 60Hz	PC10	PC8
1920x1200 60Hz	Single	20x1200 60Hz	PC10	PC8
1920x1440 60Hz	Single	20x1440 60Hz	PC10	PC8
2048x1536 60Hz	Single	48x1536 60Hz	PC10	PC8
2560x1600 60Hz	Single	60x1600 60Hz	PC10	PC8
1 of 2	Single	of 2	stined	undefine

Power Management



Table 4-7. Deepest Package C-State Available (Sheet 2 of 2)

		d une	Y/U Proces	ssor Line ^{1,2}	
	Resolution	Number of Displays	PSR Enabled	PSR Disabled	stined u
	2560x1920 60Hz	Single	PC10	PC8	nde.
	2880x1620 60Hz	Single	PC10	PC8	
	2880x1800 60Hz	Single	PC10	PC8	
ned un	3200x1800 60Hz	Single	PC10	PC8	
INE	3200*2000 60Hz	Single	PC10	PC8	
inec	3840x2160 60Hz	Single	PC10	PC8	
	4096x2160 60Hz	Single	PC10	PC8	

Notes:

The deepest C-state has variance, dependent on various parameters, such software and Platform devices. 2. 3. N/A

Integrated Memory Controller (IMC) Power Management

The main memory is power managed during normal operation and in low-power ACPI C-states.

4.3.1

Disabling Unused System Memory Outputs

Any system memory (SM) interface signal that goes to a memory in which it is not connected to any actual memory devices (such as SODIMM connector is unpopulated, or is single-sided) is tri-stated. The benefits of disabling unused SM signals are:

- Reduced power consumption.
- Reduced possible overshoot/undershoot signal quality issues seen by the processor I/O buffer receivers caused by reflections from potentially un-terminated transmission lines.

When a given rank is not populated, the corresponding control signals (CLK_P/CLK_N/ CKE/ODT/CS) are not driven.

At reset, all rows should be assumed to be populated, until it can be proven that they are not populated. This is due to the fact that when CKE is tri-stated with a DRAMs present, the DRAMs are not ensured to maintain data integrity. CKE tri-state should be enabled by BIOS where appropriate, since at reset all rows should be assumed to be populated.

DRAM Power Management and Initialization

The processor implements extensive support for power management on the memory interface.Each channel drives 4 CKE pins, one per rank.

The CKE is one of the power-saving means. When CKE is off, the internal DDR clock is disabled and the DDR power is reduced. The power-saving differs according to the selected mode and the DDR type used. For more information, refer to the IDD table in the DDR specification. in a undefined undefil



a undefined undefine The processor supports four different types of power-down modes in package C0 state. The different power-down modes can be enabled through configuring PM PDWN configuration register. The type of CKE power-down can be configured through PDWN_mode (bits 15:12) and the idle timer can be configured through PDWN idle counter (bits 11:0). The different power-down modes supported are:

- No power-down (CKE disable)
- Active power-down (CKE disable) Active power-down (CKE disable) Active power-down (APD): This mode is entered if there are open pages when de-asserting CKE. In this mode the open pages are retained. Power-saving in this mode is the lowest. Power consumption of DDR is defined to the mode is fined by tXP small number of on. on.
- **PPD/DLL-off:** In this mode the data-in DLLs on DDR are off. Power-saving in this mode is the best among all power modes. Power consumption is defined by IDD2P. Exiting this mode is defined by tXP, but also tXPDLL (10–20 according to DDR type) cycles until first data transfer is allowed. For this mode, DRAM DLL should be off.
- Precharged power-down (PPD): This mode is entered if all banks in DDR are precharged when de-asserting CKE. Power-saving in this mode is intermediate better than APD, but less than DLL-off. Power consumption is defined by IDD2P. Exiting this mode is defined by tXP. The difference from APD mode is that when waking-up, all page-buffers are empty.) The LPDDR does not have a DLL. As a result, the power savings are as good as PPD/DDL-off but will have lower exit latency and higher performance.

The CKE is determined per rank, whenever it is inactive. Each rank has an idle counter. The idle-counter starts counting as soon as the rank has no accesses, and if it expires, the rank may enter power-down while no new transactions to the rank arrives to queues. The idle-counter begins counting at the last incoming transaction arrival.

It is important to understand that since the power-down decision is per rank, the IMC can find many opportunities to power down ranks, even while running memory intensive applications; the savings are significant (may be few Watts, according to DDR specification). This is significant when each channel is populated with more ranks.

Selection of power modes should be according to power-performance or thermal tradeoff of a given system:

- When trying to achieve maximum performance and power or thermal consideration is not an issue: use no power-down
- In a system which tries to minimize power-consumption, try using the deepest power-down mode possible - PPD/DLL-off with a low idle timer value
- In high-performance systems with dense packaging (that is, tricky thermal design) the power-down mode should be considered in order to reduce the heating and avoid DDR throttling caused by the heating.

The default value that BIOS configures in PM PDWN configuration register is 6080 that is, PPD/DLL-off mode with idle timer of 0x80, or 128 DCLKs. This is a balanced setting with deep power-down mode and moderate idle timer value.

The idle timer expiration count defines the # of DCLKs that a rank is idle that causes A undefined undefined undefined entry to the selected power mode. As this timer is set to a shorter time the IMC will have more opportunities to put the DDR in power-down. There is no BIOS hook to set in a undefined undefined un



Power Management

this register. Customers choosing to change the value of this register can do it by changing it in the BIOS. For experiments, this register can be modified in real time if BIOS does not lock the IMC registers.

4.3.2.1 Initialization Role of CKE

During power-up, CKE is the only input to the SDRAM that has its level recognized (other than the reset pin) once power is applied. It should be driven LOW by the DDR controller to make sure the SDRAM components float DQ and DQS during power-up. CKE signals remain LOW (while any reset is active) until the BIOS writes to a configuration register. Using this method, CKE is ensured to remain inactive for much longer than the specified 200 micro-seconds after power and clocks to SDRAM devices are stable.

4.3.2.2 Conditional Self-Refresh

During S0 idle state, system memory may be conditionally placed into self-refresh state when the processor is in package C3 or deeper power state. Refer to Section 4.4.1.1, "Intel[®] Rapid Memory Power Management (Intel[®] RMPM)" for more details on conditional self-

refresh with Intel HD Graphics enabled.

When entering the S3 – Suspend-to-RAM (STR) state or S0 conditional self-refresh, the processor IA core flushes pending cycles and then enters SDRAM ranks that are not used by the processor graphics into self-refresh. The CKE signals remain LOW so the SDRAM devices perform self-refresh.

The target behavior is to enter self-refresh for package C3 or deeper power states as long as there are no memory requests to service.

ورون aphics into self ورون aphics into self مرود و aphics into self aphices perform self-refresh. The target behavior is to enter self-refre long as there are no memory requests t Table 4-8. Targeted Memory State Conditions

StateMemory State with Processor GraphicsMemory State with External GraphicsC0, C1, C1EDynamic memory rank power-down based on idle conditions.Dynamic memory rank power-down based on idle conditions.C3, C6, C7 or deeperIf the processor graphics engine is idle and there are no pending display requests, then enter self-refresh. Otherwise use dynamic memory rank power-down based on idle conditions.If there are no memory requests, then enter self-refresh. Otherwise use dynamic memory rank power-down based on idleS3Self-Refresh ModeSelf-Refresh ModeS4Memory power-down (contents lost)Memory power-down (contents lost)	5	e are no memory requests to service. Iemory State Conditions	Lefined L.	
C3, C6, C7 or deeperIf the processor graphics engine is idle and there are no pending display requests, then enter self-refresh. Otherwise use dynamic 	State	Memory State with Processor Graphics	Memory State with External Graphics	ndefill
deeperthere are no pending display requests, then enter self-refresh. Otherwise use dynamic memory rank power-down based on idle conditions.self-refresh. Otherwise use dynamic memory rank power-down based on idle conditions.S3Self-Refresh ModeSelf-Refresh Mode	C0, C1, C1E			J.U.
		there are no pending display requests, then enter self-refresh. Otherwise use dynamic memory rank power-down based on idle	self-refresh. Otherwise use dynamic memory	
S4 Memory power-down (contents lost) Memory power-down (contents lost)	S3	Self-Refresh Mode	Self-Refresh Mode	
	S4	Memory power-down (contents lost)	Memory power-down (contents lost)	

4.3.2.3 **Dynamic Power-Down**

Dynamic power-down of memory is employed during normal operation. Based on idle conditions, a given memory rank may be powered down. The IMC implements aggressive CKE control to dynamically put the DRAM devices in a power-down state. The processor IA core controller can be configured to put the devices in active power-down (CKE de-assertion with open pages) or precharge power-down (CKE de-assertion with all pages closed). Precharge power-down provides greater power savings but has a bigger performance impact, since all pages will first be closed before putting the devices in power-down mode.

If dynamic power-down is enabled, all ranks are powered up before doing a refresh cycle and all ranks are powered down at the end of refresh.



4.3.2.4 **DRAM I/O Power Management**

Unused signals should be disabled to save power and reduce electromagnetic interference. This includes all signals associated with an unused memory channel. Clocks, CKE, ODT and CS signals are controlled per DIMM rank and will be powered down for unused ranks.

The I/O buffer for an unused signal should be tri-stated (output driver disabled), the input receiver (differential sense-amp) should be disabled, and any DLL circuitry related ONLY to unused signals should be disabled. The input path should be gated to prevent spurious results due to noise on the unused signals (typically handled automatically when input receiver is disabled).

4.3.3 DDR Electrical Power Gating (EPG)

The DDR I/O of the processor supports Electrical Power Gating (DDR-EPG) while the processor is at C3 or deeper power state.

In C3 or deeper power state, the processor internally gates VDDQ for the majority of the logic to reduce idle power while keeping all critical DDR pins such as CKE and VREF in the appropriate state.

In C7 or deeper power state, the processor internally gates V_{CCIO} for all non-critical state to reduce idle power.

In S3 or C-state transitions, the DDR does not go through training mode and will restore the previous training information.

Indefined undefine 4.3.4 **Power Training**

BIOS MRC performing Power Training steps to reduce DDR I/O power while keeping reasonable operational margins, still ensuring platform operation. The algorithms attempt to weaken ODT, driver strength and the related buffers parameters both on the MC and the DRAM side and find the best possible trade-off between the total I/O power and the operational margins using advanced mathematical models.

Note:

ed unde

4.4 **Processor Graphics Power Management**

4.4.1Memory Power Savings Technologies

4.4.1.1

Intel[®] Rapid Memory Power Management (Intel[®] RMPM)

Intel[®] Rapid Memory Power Management (Intel[®] RMPM) conditionally places memory into self-refresh when the processor is in package C3 or deeper power state to allow the system to remain in the deeper power states longer for memory not reserved for A undefined undefined undefined graphics memory. Intel RMPM functionality depends on graphics/display state (relevant only when processor graphics is being used), as well as memory traffic patterns generated by other connected I/O devices. imod undefined undefined

Datasheet, Volume 1 of 2 Infined Unde



4.4.1.2 Intel[®] Smart 2D Display Technology (Intel[®] S2DDT)

Intel S2DDT reduces display refresh memory traffic by reducing memory reads required for display refresh. Power consumption is reduced by less accesses to the IMC. Intel S2DDT is only enabled in single pipe mode.

Intel S2DDT is most effective with:

- Display images well suited to compression, such as text windows, slide shows, and so on. Poor examples are 3D games.
- Static screens such as screens with significant portions of the background showing 2D applications, processor benchmarks, and so on, or conditions when the processor is idle. Poor examples are full-screen 3D games and benchmarks that flip the display image at or near display refresh rates.

4.4.2 **Display Power Savings Technologies**

4.4.2.1

Intel[®] (Seamless & Static) Display Refresh Rate Switching (DRRS) with eDP* Port

Intel DRRS provides a mechanism where the monitor is placed in a slower refresh rate (the rate at which the display is updated). The system is smart enough to know that the user is not displaying either 3D or media like a movie where specific refresh rates are required. The technology is very useful in an environment such as a plane where the user is in battery mode doing E-mail, or other standard office applications. It is also useful where the user may be viewing web pages or social media sites while in battery mode.

uner 3D or media ...و بوديد بين العصي بين المصي بين الم المصي بالمصي بين المصي بين المصي بالم م

Intel Automatic Display Brightness feature dynamically adjusts the backlight brightness based upon the current ambient light environment. This feature requires an additional sensor to be on the panel front. The sensor receives the changing ambient light conditions and sends the interrupts to the Intel Graphics driver. As per the change in Lux, (current ambient light illuminance), the new backlight setting can be adjusted through BLC. The converse applies for a brightly lit environment. Intel Automatic Display Brightness increases the backlight setting.

4.4.2.3 Smooth Brightness

The Smooth Brightness feature is the ability to make fine grained changes to the screen brightness. All Windows* 10 system that support brightness control are required to support Smooth Brightness control and it should be supporting 101 levels of brightness control. Apart from the Graphics driver changes, there may be few System BIOS changes required to make this feature functional.

4 Intel[®] Display Power Saving Technology (Intel[®] DPST) 6.0

The Intel DPST technique achieves backlight power savings while maintaining a good visual experience. This is accomplished by adaptively enhancing the displayed image while decreasing the backlight brightness simultaneously. The goal of this technique is to provide equivalent end-user-perceived image quality at a decreased backlight power level.

1. The original (input) image produced by the operating system or application is analyzed by the Intel DPST subsystem. An interrupt to Intel DPST software is



generated whenever a meaningful change in the image attributes is detected. (A meaningful change is when the Intel DPST software algorithm determines that enough brightness, contrast, or color change has occurred to the displaying images that the image enhancement and backlight control needs to be altered.)

- 2. Intel DPST subsystem applies an image-specific enhancement to increase image contrast, brightness, and other attributes.
- 3. A corresponding decrease to the backlight brightness is applied simultaneously to produce an image with similar user-perceived quality (such as brightness) as the original image.

Intel DPST 6.0 has improved the software algorithms and has minor hardware changes to better handle backlight phase-in and ensures the documented and validated method to interrupt hardware phase-in.

Idefined undefined 4.4.2.5 Panel Self-Refresh 2 (PSR 2)

Panel Self-Refresh feature allows the Processor Graphics core to enter low-power state panels capable of supporting Panel Self-Refresh. Apart from being able to support, the eDP* panel should be eDP 1.4 compliant PSP 2 adds as the first state of the support of the eDP 1.4 compliant PSP 2 adds as the first state of the support of th requires an eDP 1.4 compliant panel.

PSR2 is limited to 3200x2000@60 Maximum display resolution.

4.4.2.6 Low-Power Single Pipe (LPSP)

Low-power single pipe is a power conservation feature that helps save power by keeping the inactive pipes powered OFF. This feature is enabled only in a single display configuration without any scaling functionalities. This feature is supported from 4th Generation Intel[®] Core[™] processor family onwards. LPSP is achieved by keeping a single pipe enabled during eDP* only with minimal display pipeline support. This feature is panel independent and works with any eDP panel (port A) in single display mode.

Processor Graphics Core Power Savings Technologies

4.4.3.1

Intel[®] Graphics Dynamic Frequency

Intel Turbo Boost Technology 2.0 is the ability of the processor IA cores and graphics (Graphics Dynamic Frequency) cores to opportunistically increase frequency and/or voltage above the guaranteed processor and graphics frequency for the given part. Intel Graphics Dynamic Frequency is a performance feature that makes use of unused package power and thermals to increase application performance. The increase in frequency is determined by how much power and thermal budget is available in the package, and the application demand for additional processor or graphics performance. The processor IA core control is maintained by an embedded controller. The graphics driver dynamically adjusts between P-States to maintain optimal performance, power, and thermals. The graphics driver will always place the graphics engine in its lowest possible P-State. Intel Graphics Dynamic Frequency requires BIOS support. Additional power and thermal budget should be available. in a materined undefined undefined

undefined undef Datasheet, Volume 1 of 2 Infined Under



Intel[®] Graphics Render Standby Technology (Intel[®] GRST) 4.4.3.2

The final power savings technology from Intel happens while the system is asleep. This is another technology where the voltage is adjusted down. For RC6 the voltage is adjusted very low, or very close to zero, what may reduced power by over 1000.

Dynamic FPS (DFPS) 4.4.3.3

Dynamic FPS (DFPS) or dynamic frame-rate control is a runtime feature for improving power-efficiency for 3D workloads. Its purpose is to limit the frame-rate of full screen 3D applications without compromising on user experience. By limiting the frame rate, the load on the graphics engine is reduced, giving an opportunity to run the Processor Graphics at lower speeds, resulting in power savings. This feature works in both AC/DC modes.

Idefined undefine

System Agent Enhanced Intel[®] Speedstep[®] Technology

System Agent Enhanced Intel Speedstep Technology, a new feature for this processor, is dynamic voltage frequency scaling of the System Agent clock based on memory utilization. Unlike processor core and package Enhanced Intel Speedstep Technology, System Agent Enhanced Intel Speedstep Technology has only two valid operating points.

When workload is low and SA Enhanced Speedstep Technology is enabled, the DDR data rate may drop temporally as follows:

- DDR3L/LPDDR3 1066 MT/s
- DDR4 1333 MT/s

Before changing the DDR data rate, the processor sets DDR to self-refresh and changes needed parameters. The DDR voltage remains stable and unchanged.

BIOS/MRC DDR training at high and low frequencies sets I/O and timing parameters.

Voltage Optimization

undefined undefined undefined undefined undefined undefined Voltage Optimization opportunistically provides reduction in power consumption, that is, a boost in performance at a given PL1. Over time the benefit is reduced. There is no change to base frequency or turbo frequency. During system validation and tuning, this feature should be disabled to reflect processor power and performance that is expected weinen undefined undefined undefined undefined undefined over time.



5.1 **Processor Thermal Management**

The thermal solution provides both component-level and system-level thermal management. To allow optimal operation and long-term reliability of Intel processorbased systems, the system/processor thermal solution should be designed so that the processor:

- Bare Die Parts: Remains below the maximum junction temperature $(T_{j_{MAX}})$ specification at the maximum thermal design power (TDP).
- Lidded Parts: Remains below the maximum case temperature (Tcmax) specification at the maximum thermal design power.
- Conforms to system constraints, such as system acoustics, system skintemperatures, and exhaust-temperature requirements.

Caution:

Thermal specifications given in this chapter are on the component and package level and apply specifically to the processor. Operating the processor outside the specified limits may result in permanent damage to the processor and potentially other components in the system.

5.1.1 Thermal Considerations

The processor TDP is the maximum sustained power that should be used for design of the processor thermal solution. TDP is a power dissipation and component temperature operating condition limit, specified in this document, that is validated during manufacturing for the base configuration when executing a near worst case commercially available workload as specified by Intel for the SKU segment. TDP may be exceeded for short periods of time or if running a very high power workload.

To allow the optimal operation and long-term reliability of Intel processor-based systems, the processor must remain within the minimum and maximum component temperature specifications. For lidded parts, the appropriate case temperature (T_{CASE}) specifications is defined by the applicable thermal profile. For bare die parts, the component temperature specification is the applicable Tj_{MAX} .

Thermal solutions not designed to provide this level of thermal capability may affect the long-term reliability of the processor and system.

The processor integrates multiple processing IA cores, graphics cores and a PCH, or a PCH and EDRAM, on a single package. This may result in power distribution differences across the package and should be considered when designing the thermal solution.

Intel Turbo Boost Technology 2.0 allows processor IA cores to run faster than the base frequency. It is invoked opportunistically and automatically as long as the processor is conforming to its temperature, voltage, power delivery and current control limits. When Intel Turbo Boost Technology 2.0 is enabled:

Applications are expected to run closer to TDP more often as the processor will A undefined undefined undefined attempt to maximize performance by taking advantage of estimated available energy budget in the processor package. in a undefined undefined ut

Datasheet, Volume 1 of 2 Infined Under



- The processor may exceed the TDP for short durations to utilize any available thermal capacitance within the thermal solution. The duration and time of such operation can be limited by platform runtime configurable registers within the processor.
- Graphics peak frequency operation is based on the assumption of only one of the graphics domains (GT/GTx) being active. This definition is similar to the IA core Turbo concept, where peak turbo frequency can be achieved when only one IA core is active. Depending on the workload being applied and the distribution across the graphics domains the user may not observe peak graphics frequency for a given workload or benchmark.
- Thermal solutions and platform cooling that are designed to less than thermal design guidance may experience thermal and performance issues.

Intel Turbo Boost Technology 2.0 availability may vary between the different SKUs.

Intel[®] Turbo Boost Technology 2.0 Power Monitoring 5.1.2

When operating in turbo mode, the processor monitors its own power and adjusts the processor and graphics frequencies to maintain the average power within limits over a thermally significant time period. The processor estimates the package power for all components on package. In the event that a workload causes the temperature to exceed program temperature limits, the processor will protect itself using the Adaptive Thermal Monitor.

5.1.3 Intel[®] Turbo Boost Technology 2.0 Power Control

Illustration of Intel[®] Turbo Boost Technology 2.0 power control is shown in the following sections and figures. Multiple controls operate simultaneously allowing customization for multiple system thermal and power limitations. These controls allow for turbo optimizations within system constraints and are accessible using MSR, MMIO, or PECI interfaces (see the appropriate processor Turbo Implementation Guide for more information).

5.1.3.1

Note:

Package Power Control

The package power control settings of PL1, PL2, PL3, PL4 and Tau allow the designer to configure Intel Turbo Boost Technology 2.0 to match the platform power delivery and package thermal solution limitations.

- Power Limit 1 (PL1): A threshold for average power that will not exceed recommend to set to equal TDP power. PL1 should not be set higher than thermal solution cooling limits.
- Power Limit 2 (PL2): A threshold that if exceeded, the PL2 rapid power limiting algorithms will attempt to limit the spike above PL2.
- Power Limit 3 (PL3): A threshold that if exceeded, the PL3 rapid power limiting algorithms will attempt to limit the duty cycle of spikes above PL3 by reactively limiting frequency. This is an optional setting
- Power Limit 4 (PL4): A limit that will not be exceeded, the PL4 power limiting algorithms will preemptively limit frequency to prevent spikes above PL4.
- Turbo Time Parameter (Tau): An averaging constant used for PL1 exponential weighted moving average (EWMA) power calculation. timed undefined undefined

Datasheet, Volume 1 of 2 -4 undefined

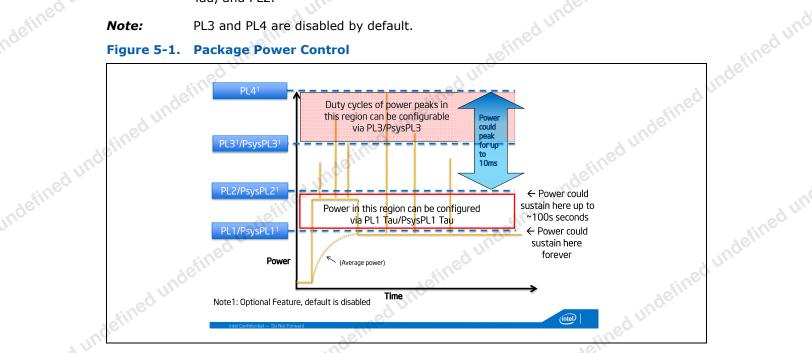


Note:

Implementation of Intel Turbo Boost Technology 2.0 only requires configuring PL1, PL1 Tau, and PL2.

PL3 and PL4 are disabled by default. Note:





5.1.3.2 **Platform Power Control**

The processor supports Psys (Platform Power) to enhance processor power management. The Psys signal needs to be sourced from a compatible charger circuit and routed to the IMVP8 (voltage regulator). This signal will provide the total thermally relevant platform power consumption (processor and rest of platform) via SVID to the processor.

When the Psys signal is properly implemented, the system designer can utilize the package power control settings of PsysPL1/Tau, PsysPL2 and PsysPL3 for additional manageability to match the platform power delivery and platform thermal solution limitations for Intel Turbo Boost Technology 2.0. The operation of the PsysPL1/tau, PsysPL2 and PsysPL3 is analogous to the processor power limits described in Section 5.1.3.1, "Package Power Control".

- Platform Power Limit 1 (PsysPL1): A threshold for average platform power that will not be exceeded - recommend to set to equal platform thermal capability.
- Platform Power Limit 2 (PsysPL2): A threshold that if exceeded, the PsysPL2 rapid power limiting algorithms will attempt to limit the spikes above PsysPL2.
- Platform Power Limit 3 (PsvsPL3): A threshold that if exceeded, the PsvsPL3 rapid power limiting algorithms will attempt to limit the duty cycle of spikes above PsysPL3 by reactively limiting frequency.
- PsysPL1 Tau: An averaging constant used for PsysPL1 exponential weighted moving average (EWMA) power calculation.
- A undefined undefined undefined The Psys signal and associated power limits / Tau are optional for the system designer and disabled by default.
- The Psys data will not include power consumption for charging.

Datasheet, Volume 1 of 2 weined undef

intel under

5.1.3.3

Turbo Time Parameter (Tau)

Turbo Time Parameter (Tau) is a mathematical parameter (units of seconds) that controls the Intel Turbo Boost Technology 2.0 algorithm. During a maximum power turbo event, the processor could sustain PL2 for a duration longer than the Turbo Time Parameter. If the power value and/or Turbo Time Parameter is changed during runtime, to settle at the new control limits. The time varies depending on the magnitude of the change, power limits, and other factors. There is an individual in change, power limits, and other factors. There is an individual Turbo Time Parameter associated with Package Power Control and Platform Power Control.

5.1.4

Configurable TDP (cTDP) and Low-Power Mode

Configurable TDP (cTDP) and Low-Power Mode (LPM) form a design option where the processor's behavior and package TDP are dynamically adjusted to a desired system performance and power envelope. Configurable TDP and Low-Power Mode technologies offer opportunities to differentiate system design while running active workloads on select processor SKUs through scalability, configuration and adaptability. The scenarios or methods by which each technology is used are customizable but typically involve changes to PL1 and associated frequencies for the scenario with a resultant change in performance depending on system's usage. Either technology can be triggered by (but are not limited to) changes in OS power policies or hardware events such as docking a system, flipping a switch or pressing a button. cTDP and LPM are designed to be configured dynamically and do not require an operating system reboot.

Configurable TDP and Low-Power Mode technologies are not battery life improvement technologies.

5.1.4.1 **Configurable TDP**

Note:

Note:

Configurable TDP availability may vary between the different SKUs.

With cTDP, the processor is now capable of altering the maximum sustained power with $^{
m O}$ an alternate processor IA core base frequency. Configurable TDP allows operation in situations where extra cooling is available or situations where a cooler and quieter mode of operation is desired. Configurable TDP can be enabled using Intel's DPTF driver or through HW/EC firmware. Enabling cTDP using the DPTF driver is recommended as Intel does not provide specific application or EC source code.

undefined undefir Table 5-1. Configurable TDP Modes (Sheet 1 of 2)

CI DP consists	of three modes as shown in the following table.	ned u
		ndefill
Mode	Description	.0
Base	The average power dissipation and junction temperature operating condition limit, specified in Table 5-2, Table 5-3 and Table 5-5 for the SKU Segment and Configuration, for which the processor is validated during manufacturing when executing an associated Intel-specified high-complexity workload at the processor IA core frequency corresponding to the configuration and SKU.	
TDP-Up	The SKU-specific processor IA core frequency where manufacturing confirms logical functionality within the set of operating condition limits specified for the SKU segment and Configurable TDP-Up configuration in Table 5-2, Table 5-3 and Table 5-5. The Configurable TDP-Up Frequency and corresponding TDP is higher than the processor IA core Base Frequency and SKU Segment Base TDP.	ed'
undefined	ne adefined under	led undefine
	Datasheet, Volume 1 of 2	2
	ed undefined un	
	Base	Mode Description Base The average power dissipation and junction temperature operating condition limit, specified in Table 5-2, Table 5-3 and Table 5-5 for the SKU Segment and Configuration, for which the processor is validated during manufacturing when executing an associated Intel-specified high-complexity workload at the processor IA core frequency corresponding to the configuration and SKU. TDP-Up The SKU-specific processor IA core frequency where manufacturing confirms logical functionality within the set of operating condition limits specified for the SKU segment and Configurable TDP-Up configuration in Table 5-2, Table 5-3 and Table 5-5. The Configurable TDP-Up Frequency and corresponding TDP is higher than the processor IA core Base Frequency and SKU Segment Base TDP.



Table 5-1. Configurable TDP Modes (Sheet 2 of 2)

Mode	Description	
TDP-Down	The processor IA core frequency where manufacturing confirms logical functionality within the set of operating condition limits specified for the SKU segment and Configurable TDP-Down configuration in Table 5-2, Table 5-3 and Table 5-5. The Configurable TDP-Down Frequency and corresponding TDP is lower than the processor IA core Base Frequency and SKU Segment Base TDP.	defined un

In each mode, the Intel Turbo Boost Technology 2.0 power limits are reprogrammed along with a new OS controlled frequency range. The DPTF driver assists in all these operations. The cTDP mode does not change the max per-processor IA core turbo frequency.

5.1.4.2 **Low-Power Mode**

Low-Power Mode (LPM) can provide cooler and quieter system operation. By combining several active power limiting techniques, the processor can consume less power while running at equivalent low frequencies. Active power is defined as processor power consumed while a workload is running and does not refer to the power consumed during idle modes of operation. LPM is only available using the Intel DPTF driver.

Thermal Management Features

Occasionally the processor may operate in conditions that are near to its maximum operating temperature. This can be due to internal overheating or overheating within the platform. In order to protect the processor and the platform from thermal failure, several thermal management features exist to reduce package power consumption and thereby temperature in order to remain within normal operating limits. Furthermore, the processor supports several methods to reduce memory power.

5.1.5.1 **Adaptive Thermal Monitor**

The purpose of the Adaptive Thermal Monitor is to reduce processor IA core power consumption and temperature until it operates below its maximum operating temperature. Processor IA core power reduction is achieved by:

- Adjusting the operating frequency (using the processor IA core ratio multiplier) and voltage.
- Modulating (starting and stopping) the internal processor IA core clocks (duty cycle).

The Adaptive Thermal Monitor can be activated when the package temperature, monitored by any digital thermal sensor (DTS), meets its maximum operating temperature. The maximum operating temperature implies maximum junction temperature Tj_{MAX}.

Reaching the maximum operating temperature activates the Thermal Control Circuit (TCC). When activated the TCC causes both the processor IA core and graphics core to reduce frequency and voltage adaptively. The Adaptive Thermal Monitor will remain active as long as the package temperature remains at its specified limit. Therefore, the Adaptive Thermal Monitor will continue to reduce the package frequency and voltage until the TCC is de-activated.

undefined undefined undefined T_{MAX} is factory calibrated and is not user configurable. The default value is software visible in the TEMPERATURE_TARGET (0x1A2) MSR, bits [23:16].



The Adaptive Thermal Monitor does not require any additional hardware, software drivers, or interrupt handling routines. It is not intended as a mechanism to maintain processor thermal control to PL1 = TDP. The system design should provide a thermal solution that can maintain normal operation when PL1 = TDP within the intended usage undefined range.

Adaptive Thermal Monitor protection is always enabled.

TCC Activation Offset 5.1.5.1.1

TCC Activation Offset can be set as an offset from the maximum allowed component temperature to lower the onset of TCC and Adaptive Thermal Monitor. In addition, the processor has added an optional time window (Tau) to manage processor performance at the TCC Activation offset value via an EWMA (Exponential Weighted Moving Average) of temperature.

TCC Activation Offset with Tau=0

An offset (degrees Celsius) can be written to the TEMPERATURE TARGET (0x1A2) MSR, bits [29:24], the offset value will be subtracted from the value found in bits [23:16]. When the time window (Tau) is set to zero, there will be no averaging, the offset, will be subtracted from the Tj_{MAX} value and used as a new max temperature set point for Adaptive Thermal Monitoring. This will have the same behavior as in prior products to have TCC activation and Adaptive Thermal Monitor to occur at this lower target silicon temperature.

If enabled, the offset should be set lower than any other passive protection such as ACPI PSV trip points

TCC Activation Offset with Tau

To manage the processor with the EWMA (Exponential Weighted Moving Average) of temperature, an offset (degrees Celsius) is written to the TEMPERATURE_TARGET (0x1A2) MSR, bits [29:24], and the time window (Tau) is written to the TEMPERATURE TARGET (0x1A2) MSR [6:0]. The Offset value will be subtracted from the value found in bits [23:16] and be the temperature.

The processor will manage to this average temperature by adjusting the frequency of the various domains. The instantaneous Tj can briefly exceed the average temperature. The magnitude and duration of the overshoot is managed by the time window value (Tau).

This averaged temperature thermal management mechanism is in addition, and not 30 unde instead of Tj_{MAX} thermal management. That is, whether the TCC activation offset is 0 or not, TCC Activation will occur at Tj_{MAX}.

Frequency / Voltage Control 5.1.5.1.2

Upon Adaptive Thermal Monitor activation, the processor attempts to dynamically reduce processor temperature by lowering the frequency and voltage operating point. The operating points are automatically calculated by the processor IA core itself and do not require the BIOS to program them as with previous generations of Intel processors. The processor IA core will scale the operating points such that:

 The voltage will be optimized according to the temperature, the processor IA core bus ratio and number of processor IA cores in deep C-states.



 The processor IA core power and temperature are reduced while minimizing performance degradation.

Once the temperature has dropped below the trigger temperature, the operating frequency and voltage will transition back to the normal system operating point.

Once a target frequency/bus ratio is resolved, the processor IA core will transition to the new target automatically.

- On an upward operating point transition the voltage transition precedes the frequency transition.
- On a downward transition the frequency transition precedes the voltage transition.
- The processor continues to execute instructions. However, the processor will halt instruction execution for frequency transitions.

If a processor load-based Enhanced Intel SpeedStep Technology/P-state transition (through MSR write) is initiated while the Adaptive Thermal Monitor is active, there are two possible outcomes:

- If the P-state target frequency is higher than the processor IA core optimized target frequency, the P-state transition will be deferred until the thermal event has been completed.
- If the P-state target frequency is lower than the processor IA core optimized target frequency, the processor will transition to the P-state operating point.

undefined und5.1.5.1.3 **Clock Modulation**

If the frequency/voltage changes are unable to end an Adaptive Thermal Monitor event, the Adaptive Thermal Monitor will utilize clock modulation. Clock modulation is done by alternately turning the clocks off and on at a duty cycle (ratio between clock "on" time and total time) specific to the processor. The duty cycle is factory configured to 25% on and 75% off and cannot be modified. The period of the duty cycle is configured to 32 microseconds when the Adaptive Thermal Monitor is active. Cycle times are independent of processor frequency. A small amount of hysteresis has been included to prevent excessive clock modulation when the processor temperature is near its maximum operating temperature. Once the temperature has dropped below the maximum operating temperature, and the hysteresis timer has expired, the Adaptive Thermal Monitor goes inactive and clock modulation ceases. Clock modulation is automatically engaged as part of the Adaptive Thermal Monitor activation when the frequency/voltage targets are at their minimum settings. Processor performance will be ned undefined decreased when clock modulation is active. Snooping and interrupt processing are performed in the normal manner while the Adaptive Thermal Monitor is active.

Clock modulation will not be activated by the Package average temperature control mechanism.

Digital Thermal Sensor 5.1.5.2

Each processor has multiple on-die Digital Thermal Sensor (DTS) that detects the processor IA, GT and other areas of interest instantaneous temperature.

Temperature values from the DTS can be retrieved through:

- A software interface using processor Model Specific Register (MSR).
- A undefined undefined undefined A processor hardware interface as described in Section 2.4, "Platform . s Environmental Control Interface (PECI)".

Datasheet, Volume 1 of 2 weined undef

When temperature is retrieved by the processor MSR, it is the instantaneous temperature of the given DTS. When temperature is retrieved using PECI, it is the average of the highest DTS temperature in the package over a 256 ms time window. Intel recommends using the PECI reported temperature for platform thermal control that benefits from averaging, such as fan speed control. The average DTS temperature may not be a good indicator of package Adaptive Thermal Monitor activation or rapid increases in temperature that triggers the Out of Specification status bit within the PACKAGE_THERM_STATUS MSR 1B1h and IA32_THERM_STATUS MSR 19Ch.

Code execution is halted in C1 or deeper C- states. Package temperature can still be monitored through PECI in lower C-states.

Unlike traditional thermal devices, the DTS outputs a temperature relative to the maximum supported operating temperature of the processor (Tj_{MAX}) , regardless of TCC activation offset. It is the responsibility of software to convert the relative temperature to an absolute temperature. The absolute reference temperature is readable in the TEMPERATURE_TARGET MSR 1A2h. The temperature returned by the DTS is an implied negative integer indicating the relative offset from T_{MAX} . The DTS does not report temperatures greater than T_{MAX} . The DTS-relative temperature readout directly impacts the Adaptive Thermal Monitor trigger point. When a package DTS indicates that it has reached the TCC activation (a reading of 0x0, except when the TCC activation offset is changed), the TCC will activate and indicate an Adaptive Thermal Monitor event. A TCC activation will lower both processor IA core and graphics core frequency, voltage, or both. Changes to the temperature can be detected using two programmable thresholds located in the processor thermal MSRs. These thresholds have the capability of generating interrupts using the processor IA core's local APIC. Refer to the Intel 64 and IA-32 Architectures Software Developer's Manual for specific register and programming details.

5.1.5.2.1 Digital Thermal Sensor Accuracy (Taccuracy)

The error associated with DTS measurements will not exceed ±5 °C within the entire operating range.

5.1.5.2.2 Fan Speed Control with Digital Thermal Sensor

intel) red under

Digital Thermal Sensor based fan speed control (T_{FAN}) is a recommended feature to achieve optimal thermal performance. At the T_{FAN} temperature, Intel recommends full cooling capability before the DTS reading reaches T_{MAX} .

5.1.5.3 **PROCHOT# Signal**

PROCHOT# (processor hot) is asserted by the processor when the TCC is active. Only a single PROCHOT# pin exists at a package level. When any DTS temperature reaches the TCC activation temperature, the PROCHOT# signal will be asserted. PROCHOT# assertion policies are independent of Adaptive Thermal Monitor enabling. is a undefined undefined undefined undefined undefined undefined

Datasheet, Volume 1 of 2

Lesined undefined undefined undefined undefined



5.1.5.4

Bi-Directional PROCHOT#

By default, the PROCHOT# signal is set to input only. When configured as an input or bi-directional signal, PROCHOT# can be used for thermally protecting other platform components should they overheat as well. When PROCHOT# is driven by an external device:

- The package will immediately transition to the lowest P-State (Pn) supported by the processor IA cores and graphics cores. This is contrary to the internally-generated Adaptive Thermal Monitor response.
- Clock modulation is not activated.

The processor package will remain at the lowest supported P-state until the system deasserts PROCHOT#. The processor can be configured to generate an interrupt upon assertion and de-assertion of the PROCHOT# signal.

When PROCHOT# is configured as a bi-directional signal and PROCHOT# is asserted by the processor, it is impossible for the processor to detect a system assertion of PROCHOT#. The system assertion will have to wait until the processor de-asserts PROCHOT# before PROCHOT# action can occur due to the system assertion. While the processor is hot and asserting PROCHOT#, the power is reduced but the reduction rate is slower than the system PROCHOT# response of < 100 us. The processor thermal control is staged in smaller increments over many milliseconds. This may cause several milliseconds of delay to a system assertion of PROCHOT# while the output function is asserted.

5.1.5.5 Voltage Regulator Protection using PROCHOT#

PROCHOT# may be used for thermal protection of voltage regulators (VR). System designers can create a circuit to monitor the VR temperature and assert PROCHOT# and, if enabled, activate the TCC when the temperature limit of the VR is reached. When PROCHOT# is configured as a bi-directional or input only signal, if the system assertion of PROCHOT# is recognized by the processor, it will result in an immediate transition to the lowest P-State (Pn) supported by the processor IA cores and graphics cores. Systems should still provide proper cooling for the VR and rely on bi-directional PROCHOT# only as a backup in case of system cooling failure. Overall, the system thermal design should allow the power delivery circuitry to operate within its temperature specification even while the processor is operating at its TDP.

undefined und Thermal Solution Design and PROCHOT# Behavior 5.1.5.6

With a properly designed and characterized thermal solution, it is anticipated that PROCHOT# will only be asserted for very short periods of time when running the most power intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be so minor that it would be immeasurable. However, an under-designed thermal solution that is not able to prevent excessive assertion of PROCHOT# in the anticipated ambient environment may:

- Cause a noticeable performance loss.
- Result in prolonged operation at or above the specified maximum junction temperature and affect the long-term reliability of the processor.
- A undefined undefined undefined May be incapable of cooling the processor even when the TCC is active continuously (in extreme situations). undefined undefined un



5.1.5.7

Low-Power States and PROCHOT# Behavior

Depending on package power levels during package C-states, outbound PROCHOT# may de-assert while the processor is idle as power is removed from the signal. Upon wake up, if the processor is still hot, the PROCHOT# will re-assert. Although, typically package idle state residency should resolve any thermal issues. The PECI interface is fully operational during all C-states and it is expected that the platform continues to manage processor IA core and package thermals even during idle states by regularly polling for thermal data over PECI.

5.1.5.8 **THERMTRIP#** Signal

Regardless of enabling the automatic or on-demand modes, in the event of a catastrophic cooling failure, the package will automatically shut down when the silicon has reached an elevated temperature that risks physical damage to the product. At this point, the THERMTRIP# signal will go active.

5.1.5.9 **Critical Temperature Detection**

Critical Temperature detection is performed by monitoring the package temperature. This feature is intended for graceful shutdown before the THERMTRIP# is activated. However, the processor execution is not guaranteed between critical temperature and THERMTRIP#. If the Adaptive Thermal Monitor is triggered and the temperature remains high, a critical temperature status and sticky bit are latched in the PACKAGE THERM STATUS MSR 1B1h and the condition also generates a thermal interrupt, if enabled. For more details on the interrupt mechanism, refer to the Intel® 64 and IA-32 Architectures Software Developer's Manual (Related Documents section).

undefined undefine 5.1.5.10 **On-Demand Mode**

The processor provides an auxiliary mechanism that allows system software to force the processor to reduce its power consumption using clock modulation. This mechanism is referred to as "On-Demand" mode and is distinct from Adaptive Thermal Monitor and bi-directional PROCHOT#. The processor platforms should not rely on software usage of this mechanism to limit the processor temperature. On-Demand Mode can be accomplished using processor MSR or chipset I/O emulation. On-Demand Mode may be used in conjunction with the Adaptive Thermal Monitor, However, if the system software tries to enable On-Demand mode at the same time the TCC is engaged, the factory configured duty cycle of the TCC will override the duty cycle selected by the On-Demand mode. If the I/O based and MSR-based On-Demand modes are in conflict, the duty cycle selected by the I/O emulation-based On-Demand mode will take precedence over the MSR-based On-Demand Mode.

5.1.5.11 **MSR Based On-Demand Mode**

If Bit 4 of the IA32_CLOCK_MODULATION MSR is set to 1, the processor will immediately reduce its power consumption using modulation of the internal processor IA core clock, independent of the processor temperature. The duty cycle of the clock modulation is programmable using bits [3:1] of the same IA32_CLOCK_MODULATION MSR. In this mode, the duty cycle can be programmed in either 12.5% or 6.25% increments (discoverable using CPUID). Thermal throttling using this method will modulate each processor IA core's clock independently.

Datasheet, Volume 1 of 2 -4 undefined



5.1.5.12 I/O Emulation-Based On-Demand Mode

I/O emulation-based clock modulation provides legacy support for operating system undefined un software that initiates clock modulation through I/O writes to ACPI defined processor clock control registers on the chipset (PROC_CNT). Thermal throttling using this method will modulate all processor IA cores simultaneously.

Intel[®] Memory Thermal Management 5.1.6

The processor provides thermal protection for system memory by throttling memory traffic when using either DIMM modules or a memory down implementation. Two levels of throttling are supported by the processor, either a warm threshold or hot threshold that is customizable through memory mapped I/O registers. Throttling based on the warm threshold should be an intermediate level of throttling. Throttling based on the hot threshold should be the most severe. The amount of throttling is dynamically controlled by the processor.

The on Die Thermal Sensor (ODTS) uses a physical thermal sensor on DRAM dies. ODTS is available for DDR4 and LPDDR3. It is used to set refresh rate according to DRAM temperature.

The memory controller reads LPDDR3 MR4 or DDR4 MR3 and configures the DDR refresh rate accordingly.

When using ODTS, the memory controller gets a Warm/Hot/Cold indication from DRAMs On-Die TS and throttles DDR accordingly. This is a method of Closed Loop Thermal Management (CLTM). Refer to document 604677 for more details on closed loop thermal management.

Memory temperature may be acquired through an on-board thermal sensor (TS-on-Board), retrieved by an embedded controller and reported to the processor through the PECI 3.1 interface. This methodology is known as PECI injected temperature. This is a method of Closed Loop Thermal Management (CLTM).

Scenario Design Power (SDP)

SDP requires that the POWER_LIMIT_1 (PL1) to be set to the cooling level capability (SDP level, or higher). While the SDP specification is characterized at Tj of 80 °C, the functional limit for the product remains at Tj_{MAX} . Customers may choose to program the TCC Offset to have TCC Activation at 80 °C, but it is not required.

The processors that have SDP specified can still exceed SDP under certain workloads, such as TDP workloads. TDP power dissipation is still possible with the intended usage models, and protection mechanisms to handle levels beyond cooling capabilities are recommended. Intel recommends using such thermal control mechanisms to manage situations where power may exceed the thermal design capability.

Note:

Note:

cTDP-Down mode is required for Intel Core products in order to achieve SDP.

Although SDP is defined at 80 °C, the TCC activation temperature is Tj_{MAX}. in a undefined undefined undefined

(intel) red undermo ndefined und 5.2

Ned undefined undefined **Thermal and Power Specifications**

(Intel)	Aerine	Thermal Management
cine lui	d uno-	Inden
5.2 The	rmal and Power Specification	ns ined v
	llowing notes apply only to Table 5.2 and Table 5-	761.
Note	Definition	,~
odefitie	The TDP and Configurable TDP values are the average power operating condition limit, for the SKU Segment and Configurat during manufacturing when executing an associated Intel-spe processor IA core frequency corresponding to the configuration	ion, for which the processor is validated cified high-complexity workload at the
ed 111 2	TDP workload may consist of a combination of processor IA co applications.	re intensive and graphics core intensive
Jefine 3	Can be modified at runtime by MSR writes, with MMIO and wi	th PECI commands.
ndefined und 2 3 4 5	'Turbo Time Parameter' is a mathematical parameter (units of turbo algorithm using a moving average of energy usage. Do value less than 0.1 seconds. refer to Section 5.1.3.2, "Platform	not set the Turbo Time Parameter to a
5	Shown limit is a time averaged power, based upon the Turbo T may exceed the set limits for short durations or under virus o	
6	Processor will be controlled to specified power limit as describ Technology 2.0 Power Monitoring". If the power value and/or 'Turbo' runtime, it may take a short period of time (approximately 3 f for the algorithm to settle at the new control limits.	ed in Section 5.1.2, "Intel ^{® Turbo Boost} Time Parameter' is changed during to 5 times the 'Turbo Time Parameter')
d une	This is a hardware default setting and not a behavioral charac code may override the hardware default power limit values to	
stinet 8	For controllable turbo workloads, the PL2 limit may be exceed	led for up to 10 ms.
inde. 9	Refer to Table 5-1, "Configurable TDP Modes" for the definition Down'.	ns of 'base'base, 'TDP-Up' and 'TDP-
undefined un 7 8 9 10	LPM power level is an opportunistic power and is not a guarar implementations may vary.	teed value as usages and
11	Power limits may vary depending on if the product supports the Default power limits can be found in the PKG_PWR_SKU MSR	
12	The processor die and OPCM die do not reach maximum susta sum of the 2 dies estimated power budget is controlled to be (PL1) limit.	
sined un 13	cTDP down power is based on GT2 equivalent graphics configuent the number of active Processor Graphics EUs, but relies on Po achieve the specified power level.	
indell' 14	May vary based on SKU.	AN ^{CO}
16	Sustained residencies at high voltages and temperatures may	temporarily limit turbo frequency.
14 16 17	Sustained residencies at high voltages and temperatures may The formula of PL2=PL1*1.25 is the hardware default but mar processor performance. By including the benefits available from power and thermal m value for PL2 found in the Power Map can be higher.	y not represent the optimum value for anagement features the recommended
undefined undefi	By including the benefits available from power and thermal m value for PL2 found in the Power Map can be higher.	4 UM
under	define	ofineo
	ad un-	unde
nden	1.efine-	
d un	unoc	detti
		d'un
	nden	efine
	dui.	
	ine	-d ul
, unde	detti	afinec
92 sined	ad un	Datasheet, Volume 1 of 2
nden	Lefiner	
dun	Inde	defini
		4 Un



Ement KBL U/Y Processor Line Thermal and Power 5.2.1 **Specifications**

5.2.1 Table 5-2.	TDP Specif	fications (KBL	U/Y/AML-Y	22 Processor	ے۔ Line)	1	1
Segment and Package	Processor IA Cores, Graphics Configuration and TDP	Configuration	Processor IA Core Frequency	Graphics core Frequency	Thermal Design Power (TDP) [w]	Scenario Design Power (SDP) [w]	Notes
efinet		Configurable TDP-Up	2.7 GHz to 2.9 GHz		25	ed unt	
U- Processor Line BGA	2 Core GT2	Base	2.4 GHz to 2.7 GHz	900 MHz to 1.1 GHz	15	N/A	1,9,10,
	15W	Configurable TDP-Down / LFM	800 MHz		7.5		11,16
	nu.	LPM	400 MHz	300 MHz	~7		
	stined	Configurable TDP-Up	1.8 GHz to 2.1 GHz	uned un	25		L L
U- Processor Line BGA	4 Core GT2 15W	Base	1.8 GHz to 2.5 GHz	900 MHz to 1.15 GHz	15	N/A	1,9,10, 11,12,16
(U-4 Core)		Configurable TDP-Down / LFM	800 MHz		10	od uno	11,12,10
0.0		LPM	400 MHz	300 MHz	~9	sine	
Y-		Configurable TDP-Up	1.6 GHz		Zinor		
Processor	2 Core GT2 4.5W	Base	1.0 GHz to 1.3 GHz	300 MHz to 1.05 GHz	4.5	3.0	1,9,10, 11,16,17
Line BGA		Configurable TDP-Down	600 MHz	od unos	3.75		11,10,17
		LFM	400 MHz	100 MHz	~3.75		ed '
Y- Processor	2 Corre CT2	Base	1.3 GHz to 1.5 GHz	300 MHz to	6	in the second	
Line BGA	2 Core GT2 6W	Configurable TDP-Down	600 MHz	850 MHz	4.5	N/A	1,9,10, 11,16,17
		LFM	400 MHz	100 MHz	~3.75	ei	
AML-Y Processor		Configurable TDP-Up	1.6 GHz		eg un		
Line BGA	2 Core GT2 5W	Base	1.1 GHz to 1.5 GHz	900 MHz to 1.05GHz	5	N/A	1,9,10, 11,16,17
	5W	Configurable TDP-Down	600 MHz	sined u.	3.5		6
	unu	LFM	400 MHz	300 MHz	~3.5		actine
Note:	The ~ sign	stands for app	roximation.			A UN	
			defin			stines	
Note:		ed un			, ur	00	
		define			sineo		
	6	un		ind	0		
	define	stands for app		300 MHz		ndefined	
Datasheet, Vo	dume 1 of 2		77.	qe.			define
						-00	n - 33
			10 ¹			- B-	

ndefined undefined TDP Specifications (KBL U/Y/AML-Y22 Processor Line) Table 5-2.



ned un	Segment and Package	Processor IA Cores, Graphics Configuration and TDP	Parameter	Min.	Hardware Default	Max	Units	Notes	efine
	U- Processor Line BGA	2-Core GT3 28W with OPC	Power Limit 1 Time (PL1 Tau) Power Limit 1 (PL1) Power Limit 2 (PL2)	0.01 N/A N/A	1 28 1.25*28	448 N/A N/A	s W W	3,4,5,6,7, 8,14,17	nde
	U- Processor Line BGA	2- Core GT3 15W with OPC	Power Limit 1 Time (PL1 Tau) Power Limit 1 (PL1) Power Limit 2 (PL2)	0.01 N/A N/A	1 15 1.25*15	448 N/A N/A	s W W	3,4,5,6,7, 8,14,17	
ined un	U- Processor Line BGA	2-Core GT2 15W	Power Limit 1 Time (PL1 Tau) Power Limit 1 (PL1) Power Limit 2 (PL2)	0.01 N/A N/A	1 15 1.25*15	448 N/A N/A	s W W	3,4,5,6,7, 8,14,17	
	U- Processor Line BGA (U-4 Core)	4-Core GT2 15W	Power Limit 1 Time (PL1 Tau) Power Limit 1 (PL1) Power Limit 2 (PL2)	0.01 N/A N/A	1 15 1.25*15	448 N/A N/A	s W W	3,4,5,6,7, 8,14,17	undefin
	Y- Processor Line BGA	2-Core GT2 ~4.5W	Power Limit 1 Time (PL1 Tau) Power Limit 1 (PL1) Power Limit 2 (PL2)	0.01 N/A N/A	1 4.5 1.25*4.5	448 N/A N/A	s W W	3,4,5,6,7, 8,14,17	
ed u	AML-Y Processor Line BGA	2-Core GT2 5W)	Power Limit 1 Time (PL1 Tau) Power Limit 1 (PL1) Power Limit 2 (PL2)	0.01 N/A N/A	1 5 1.25*5	448 N/A N/A	s W W	3,4,5,6,7, 8,14,17	
ine	Note: No S	Specifications for Mir	n/Max PL1/PL2 values, refer PAG (Pow	er Arch Guide)	for PL1/PL2 r	ecommend	ation.		

atimed undefined undefined Table 5-3. Package Turbo Specifications (KBL U/Y and AML-Y22 Processor Line)

Junction Temperature Specifications (KBL U/Y and AML-Y22 Processor Line) Table 5-4.

	tions for Mi	Power Limit 2 (PL2)		IN/A	1.25*5		VV		
		n/Max PL1/PL2 values, refe			stine			Line)	defined
Segment	Symbol	Package Turbo	Temperat	ture Range		ecification Iture Range	Units	Notes	Unc
ed un		Parameter	Min	Max	Min	Max		Jeffi	
U/U- 4 Core Processor Line BGA	Т _ј	Junction temperature limit	neo	100	35	100	e o c	1, 2	
U-Processor Line + OPC BGA	Тj	Junction temperature limit	0	100	35	100	٥C	1, 2	
Y-Processor Line BGA	Т _ј	Junction temperature limit	0	100	N/A	90	٥C	1, 2, 3	sined
AML-Y22 Processor Line BGA	Tj	Junction temperature limit	0	100	N/A	90	٥C	1, 2, 3	unden

Notes:

The thermal solution needs to ensure that the processor temperature does not exceed the TDP Specification Temperature. 1. The processor junction temperature is monitored by Digital Temperature Sensors (DTS). For DTS accuracy, refer to Section 2.

For this SKU to be specification compliance to the 90 °C TDP specification temperature, TCC Offset = 10 and Tau value 3. should be programed into MSR 1A2h. The recommended TCC Offset averaging Tau value is 5s. Refer to the Volume 2 for additional details.

e - A modefined undefined undefined

Datasheet, Volume 1 of 2 -4 undefined



Signal Description

This chapter describes the processor signals. They are arranged in functional groups according to their associated interface or category. The notations in the following table are used to describe the signal type.

The signal description also includes the type of buffer used for the particular signal (see the following table).

und Table 6-1. Signal Tables Terminology

afined un	Notation	Signal Type	
18fint	I	Input pin	un ^c
unor	0	Output pin	ned t
	I/O	Bi-directional Input/Output pin	Aefil'
	SE	Single Ended Link	no
de	Diff	Differential Link	
dun	CMOS	CMOS buffers. 1.05V- tolerant	
defined undefined un	OD	Open Drain buffer	
nder	DDR3L/-RS	DDR3L/DDR3L-RS buffers: 1.35V-tolerant	
d un	DDR3L/-RS	DDR3L/DDR3L-RS buffers: 1.35V-tolerant	
since	LPDDR3	LPDDR3 buffers: 1.2V- tolerant	
nder	DDR4	DDR4 buffers: 1.2V-tolerant	d ui
	A d unos	Analog reference or output. May be used as a threshold voltage or for buffer compensation	define
	GTL	Gunning Transceiver Logic signaling technology	une
	Ref	Voltage reference signal	
d ^u	Availability	Signal Availability condition - based on segment, SKU, platform type or any other factor	
afine	Asynchronous ¹	Signal has no timing relationship with any reference clock.	
d unde	Note: 1. Qualifier for a b	puffer type.	

Jundefined undefined und

undefinee		stem Memory Interface	f 2)	defined	unc		defined
	Signal Name	Description	Dir.	Buffer Type	Link Type		UNC
	DDR0_DQ[63:0] DDR1_DQ[63:0]	Data Buses: Data signals interface to the SDRAM data buses.	I/O	DDR3L	SE	All Processor Lines	
sined u	DDR0_DQSP[7:0] DDR0_DQSN[7:0] DDR1_DQSP[7:0] DDR1_DQSN[7:0]	Data Strobes: Differential data strobe pairs. The data is captured at the crossing point of DQS during read and write transactions.	I/O	DDR3L	Diff	All Processor Lines	
d unde.	Datasheet, Volume 1 of	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	ed u	ndefine	, un	Befined underine	undefined





red undefined undefined

(intel)	undefilit				Signal Description	
Table 6-2. DDR	R3L/-RS Memory Interface (Sheet 2 o	of 2)			nedune	
Signal Name	Description	Dir.	Buffer Type	Link Type	Availability	
DDR0_CKN[1:0] DDR0_CKP[1:0] DDR1_CKN[1:0] DDR1_CKP[1:0]	SDRAM Differential Clock: Differential clocks signal pairs, pair per rank. The crossing of the positive edge of DDR0_CKP/DDR1_CKP and the negative edge of their complement DDR0_CKN / DDR1_CKN are used to sample the command and control signals on the SDRAM.	ue,d	DDR3L	Diff	[1:0] applicable for all Processor Lines.	ndefi
DDR0_CKE[1:0] DDR1_CKE[1:0]	 Clock Enable: (1 per rank). These signals are used to: Initialize the SDRAMs during power-up. Power-down SDRAM ranks. Place all SDRAM ranks into and out of self-refresh during STR (Suspend to RAM). 	0	DDR3L	SE	[1:0] applicable for all Processor Lines.	
DDR0_CS#[1:0] DDR1_CS#[1:0]	Chip Select: (1 per rank). These signals are used to select particular SDRAM components during the active state. There is one Chip Select for each SDRAM rank.	0	DDR3L	SE	[1:0] applicable for all Processor Lines.	
DDR0_ODT[1:0] DDR1_ODT[1:0]	On Die Termination: (1 per rank). Active SDRAM Termination Control.	o un	DDR3L	SE	[0] applicable for all Processor Lines. [1:0] applicable for U/ U-4 Core Processor Lines.	unde
DDR0_MA[15:0] DDR1_MA[15:0] DDR0_BA[2:0] DDR1_BA[2:0]	 Memory Address: These signals are used to provide the multiplexed row and column address to the SDRAM. A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. HIGH: Autoprecharge; LOW: no Autoprecharge; LOW: no Autoprecharge. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses. A12 is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. HIGH: no burst chop; LOW: burst chopped. 	o	defined DDR3L	SE	All Processor Lines	unde
DDR0_BA[2:0] DDR1_BA[2:0]	Bank Select: These signals define which banks are selected within each SDRAM rank.	0	DDR3L	SE	All Processor Lines	ind
DDR0_CAS# DDR1_CAS#	CAS Control Signal: Column Address Select command signal	0	DDR3L	SE	All Processor Lines	ind
DDR0_RAS# DDR1_RAS#	RAS Control Signal: Row Address Select command signal	0	DDR3L	SE	All Processor Lines	9
DDR0_WE# DDR1_WE#	WE Control Signal: Write Enable command signal	0	DDR3L	SE	All Processor Lines	
DDR0_VREF_DQ DDR1_VREF_DQ	Memory Reference Voltage for DQ:	0	А	SE	All Processor Lines	
DDR1_VREF_DQ DDR_VREF_CA	Memory Reference Voltage for Command & Address:	0	A	SE	All Processor Lines	
X	efined unor	ined	undefin			ed un
96 ed undefined und	terined under				Datasheet, Volume 1 of 2	
ed u.	and unor			ل ا	ndei	



Table 6-3.

Signal Description					
etined unoe	sined undefin				intel
Table 6-3. LPD Signal Name	DR3 Memory Interface Description	Dir.	Buffer Type	Link Type	Availability
DDR0_DQ[63:0] DDR1_DQ[63:0]	Data Buses: Data signals interface to the SDRAM data buses.	I/O	LPDDR3	SE	All Processor Lines
DDR0_DQSP[7:0] DDR0_DQSN[7:0] DDR1_DQSP[7:0] DDR1_DQSN[7:0]	Data Strobes: Differential data strobe pairs. The data is captured at the crossing point of DQS during read and write transactions.	I/O	LPDDR3	Diff	All Processor Lines
DDR0_CKN[1:0] DDR0_CKP[1:0] DDR1_CKN[1:0] DDR1_CKP[1:0]	SDRAM Differential Clock: Differential clocks signal pairs, pair per rank. The crossing of the positive edge of DDR0_CKP/DDR1_CKP and the negative edge of their complement DDR0_CKN / DDR1_CKN are used to sample the command and control signals on the SDRAM.	0	LPDDR3	Diff	All Processor Lines
DDR0_CKE[3:0] DDR1_CKE[3:0]	 Clock Enable: (1 per rank) These signals are used to: Initialize the SDRAMs during power-up. Power-down SDRAM ranks. Place all SDRAM ranks into and out of self-refresh during STR. 	UIPOIE	LPDDR3	SE	All Processor Lines.
DDR0_CS#[1:0] DDR1_CS#[1:0]	Chip Select: (1 per rank). These signals are used to select particular SDRAM components during the active state. There is one Chip Select for each SDRAM rank.	0	LPDDR3	SE	All Processor Lines
DDR0_ODT[3:0] DDR1_ODT[3:0]	On Die Termination: Active Termination Control.	٥	LPDDR3	ndefi SE	For LPDDR3 only ODT[0] is in use. [0] applicable for Y- Processor Lines. [1:0] applicable for U and U- 4 Core Processor Line.
DDR0_CAA[9:0] DDR1_CAA[9:0]	Command Address: These signals are used to provide the multiplexed command and address to the SDRAM.	0	LPDDR3	SE	All Processor Lines
DDR0_CAB[9:0] DDR1_CAB[9:0]	Command Address: These signals are used to provide the multiplexed command and address to the SDRAM.	0	LPDDR3	SE	All Processor Lines
DDR0_VREF_DQ DDR1_VREF_DQ	Memory Reference Voltage for DQ:	о	A	SE	All Processor Lines
DDR_VREF_CA	Memory Reference Voltage for Command & Address:	0	Aed	SE	All Processor Lines

Table 6-4. DDR4 Memory Interface (Sheet 1 of 3)

UN				16,11			cineu
	Table 6-4. DDR	4 Memory Interface (Sheet 1 of 3)	nu.	0-			delli
	Signal Name	Description	Dir.	Buffer Type	Link Type	Availability	
	DDR0_DQ[63:0] DDR1_DQ[63:0]	Data Buses: Data signals interface to the SDRAM data buses.	I/O	DDR4	SE	All Processor Lines	
afined	DDR0_DQSP[7:0] DDR0_DQSN[7:0] DDR1_DQSP[7:0] DDR1_DQSN[7:0]	Data Strobes: Differential data strobe pairs. The data is captured at the crossing point of DQS during read and write transactions.	I/O	DDR4	Diff	All Processor Lines	
unde	20	ined undefin	ed ut	ndefine			Jundefined
	Datasheet, Volume 1 of	2 adefined under				offined underine	
1.efined		ined une			d und		



Signal Description

She undefined undefined

intel	ed undefines				Signal Description	
Table 6-4. I Signal Name	DDR4 Memory Interface (Sheet 2 of 3) Description	Dir.	Buffer Type	Link Type	Availability	
DDR0_CKN[1:0] DDR0_CKP[1:0] DDR1_CKN[1:0] DDR1_CKP[1:0]	SDRAM Differential Clock: Differential clocks signal pairs, pair per rank. The crossing of the positive edge of DDR0_CKP/DDR1_CKP and the negative edge of their complement DDR0_CKN / DDR1_CKN are used to sample the command and control signals on the SDRAM.	uod	DDR4	Diff	[1:0] applicable for All Processor Lines.	ndefin
DDR0_CKE[1:0] DDR1_CKE[1:0]	 Clock Enable: (1 per rank). These signals are used to: Initialize the SDRAMs during power-up. Power-down SDRAM ranks. Place all SDRAM ranks into and out of self-refresh during STR (Suspend to RAM). 	ο	DDR4	SE	[1:0] applicable for All Processor Lines.	
DDR0_CS#[1:0] DDR1_CS#[1:0]	Chip Select: (1 per rank). These signals are used to select particular SDRAM components during the active state. There is one Chip Select for each SDRAM rank.	0	DDR4	SE	[1:0] applicable for All Processor Lines.	
DDR0_ODT[1:0] DDR1_ODT[1:0]	On Die Termination: (1 per rank). Active SDRAM Termination Control.	0	DDR4	SE	[0] applicable for Y- ProcessorLines.[1:0] applicable for U and U- 4 Core Line processors	undefil
DDR0_MA[16:0] DDR1_MA[16:0]	 Address: These signals are used to provide the multiplexed row and column address to the SDRAM. A[16:14] use also as command signals, see ACT# signal description. A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses. A12 is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. HIGH, no burst chop; LOW: burst chopped). 	00	DDR4	SE	All Processor Lines	undef
DDR0_ACT# DDR1_ACT#	Activation Command: ACT# HIGH along with CS# determines that the signals addresses below have command functionality. A16 use as RAS# signal A15 use as CAS# signal A14 use as WE# signal	ed u	DDR4	SE	All Processor Lines	d unde
DDR0_BG[1:0] DDR1_BG[1:0]	 Bank Group: BG[0:1] define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. 	0	DDR4	SE	All processor lines SO-DIMM, x8 DRAMs, x16 DDP DRAMs devices use BG[1:0]. x16 SDP DRAMs devices use BG[0]	
DDR0_BA[1:0] DDR1_BA[1:0]	Bank Address: BA[1:0] define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.	0	DDR4	SE	All Processor Lines	
98 98 undefined U	ndefined L	ined	JULC	[Datasheet, Volume 1 of 2	ed und
stineo	ned un				noc	



ed undefined undefined Table 6-4. DDR4 Memory Interface (Sheet 3 of 3)

inde	Table 6-4. DDR	4 Memory Interface (Sheet 3 of 3)				d une
stined L.	Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
nde	DDR0_ALERT# DDR1_ALERT#	Alert: This signal is used at command training only. It is getting the Command and Address Parity error flag during training. CRC feature is not supported.	Jef	DDR4	SE	All Processor Lines
	DDR0_PAR DDR1_PAR	Command and Address Parity: These signals are used for parity check.	0	DDR4	SE	All Processor Lines
	DDR_VREF_CA	Memory Reference Voltage for Command & Address:	0	А	SE	All Processor Lines

System Memory Reference and Compensation Signals

	DDR_VREF_CA	Memory Reference Voltage for Command & Address:	0	А	SE	All Processor Lines
nd	Table 6-5. Syst	em Memory Reference and Compensa	ation	Signals	cit	led un.
sined u	Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
Ider	DDR_RCOMP[2:0]	System Memory Resistance Compensation:	N/A	ANIA	SE	All Processor Lines
	OPC_RCOMP	On-Package Cache resistance Compensation from processor: Unconnected for Processors without OPC.	N/A	A	SE	Processors w/ on- package cache
	OPCE_RCOMP	On-Package Cache resistance Compensation from OPC: Unconnected for Processors without OPC.	N/A	A	SE	Processors w/ on- package cache
ed un	DDR_VTT_CNTL	System Memory Power Gate Control: When signal is high – platform memory VTT regulator is enable, output high. When signal is low - Disables the platform memory VTT regulator in C8 and deeper and S3.	0	CMOS	SE	All Processor Lines

6.2 **Reset and Miscellaneous Signals**

Table 6-6. Reset and Miscellaneous Signals (Sheet 1 of 2)

	Signal Name	Description	Dir.	Buffer Type	Link Type	Availability	
	defines	Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Intel recommends placing test points on the board for CFG pins.			10	aned und	
a undefined un	CFG[19:0]	 CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted: 1 = (Default) Normal Operation; No stall. 0 = Stall. CFG[1]: Reserved configuration lane. 	I	defined	SE	All Processor Lines.	Jefined u
. 0	ndefined undefin	 CFG[2]: Reserved CFG[3]: Reserved configuration lane. CFG[4]: eDP enable: 1 = Disabled. 0 = Enabled. CFG[6:5]: Reserved CFG[7]: Reserved CFG[19:8]: Reserved configuration lanes. 	90,		J	stined undefined	unoc
sineo	CFG_RCOMP	Configuration Resistance Compensation	N/A	N/A	SE	All Processor Lines	
unden.	PROC_POPIRCOMP	POPIO Resistance Compensation	N/A	N/A	SE	Y and U/U- 4 Core Processor Line	ined i
20 °	Datasheet, Volume 1 of 2	ned un	ed u	nor		etined undefine	d undefit.
Jefineo		ined un			d un		



Signal Description

Reset and Miscellaneous Signals (Sheet 2 of 2) Table 6-6.

Table 6-6. R	eset and Miscellaneous Signals (Sheet 2	of 2))		ned undefill.
Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
PROC_SELECT#	Processor Select: This pin is for compatibility with future platforms. It should be unconnected for this processor.	60.	stinet	N/A	All Processor Lines

embedded DisplayPort* (eDP*) Signals 6.3

Table 6-7. embedded DisplayPort* Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DP_TXP[3:0] DP_TXN[3:0]	embedded DisplayPort Transmit: differential pair	0	eDP	Diff	All Processor Lines
DP_AUXP DP_AUXN	embedded DisplayPort Auxiliary: Half-duplex, bidirectional channel consist of one differential pair.	0	eDP	Diff	All Processor Lines
DP_DISP_UTIL	embedded DisplayPort Utility: Output control signal used for brightness correction of embedded LCD displays with backlight modulation. This pin will co-exist with functionality similar to existing BKLTCTL pin on PCH	0	Async CMOS	SE	All Processor Lines
DP_RCOMP	DDI IO Compensation resistor, supporting DP*, eDP* and HDMI* channels.	N/A	А	SE	All Processor Lines

undefined u **Display Interface Signals** 6.4

Table 6-8. Display Interface Signals

6.4 D	isplay	Interface Signals			UNO		
Table 6-8. Dis	splay Inte	erface Signals		1 etineu			sined u.
Signal Name	eined ur	Description	Dir.	Buffer Type	Link Type	Availability ⁽²⁾	undeth
DDI1_TXP[3:0] DDI1_TXN[3:0] DDI2_TXP[3:0] DDI2_TXN[3:0]		gital Display Interface Transmit: fferential Pairs	ο	DP/ HDMI*	Diff	All Processor Lines.	
DDI1_AUXP DDI1_AUXN DDI2_AUXP DDI2_AUXN	Au	gital Display Interface Display Port uxiliary: Half-duplex, bidirectional annel consist of one differential pair for ch channel.	ο	DP/ HDMI*	Diff	etinec	
Notor		10 ¹¹		11:5		•	. 6

Note:

Testability Signals 6.5

Testability Signals (Sheet 1 of 2) Table 6-9.

	estability Signals				undefit
Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
BPM#[3:0]	Breakpoint and Performance Monitor Signals: Outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance.	I/O	GTL	SE	All Processor Lines
	defined	ined	uno		
100	d unde				Datasheet, Volume 1 of



	signal Description	ed undefine				Inter	
inde	Table 6-9. Te	estability Signals (Sheet 2 of 2)					
stined u.	Signal Name	Description	Dir.	Buffer Type	Link Type	Availability	inde
NOT	PROC_PRDY#	Probe Mode Ready: PROC_PRDY# is a processor output used by debug tools to determine processor debug readiness.	00	OD	SE	All Processor Lines	lefined L.
	PROC_PREQ#	Probe Mode Request: PROC_PREQ# is used by debug tools to request debug operation of the processor.	I	GTL	SE	All Processor Lines	NOC
2	PROC_TCK	Test Clock: This signal provides the clock input for the processor Test Bus (also known as the Test Access Port). This signal should be driven low or allowed to float during power on Reset.	I	GTL	SE	All Processor Lines	
sined un	PROC_TDI	Test Data In: This signal transfers serial test data into the processor. This signal provides the serial input needed for JTAG specification support.	I	GTL	SE	All Processor Lines	50
Inden	PROC_TDO	Test Data Out: This signal transfers serial test data out of the processor. This signal provides the serial output needed for JTAG specification support.	0	OD	SE	All Processor Lines	sofined un.
	PROC_TMS	Test Mode Select: A JTAG specification support signal used by debug tools.	I	GTL	SE	All Processor Lines	nde
	PROC_TRST#	Test Reset: Resets the Test Access Port (TAP) logic. This signal should be driven low during power on Reset.	I	GTL	SE	All Processor Lines]

red undefined undefined Testability Signals (Sheet 2 of 2)

Error and Thermal Protection Signals

Table 6-10. Error and Thermal Protection Signals

	PROC_TRST#	This signal should be driven low during power on Reset.	I	GTL	SE	All Processor Lines	
	Jefin	stinet				ed us	_
ed un		rror and Thermal Protecti	on	Signa	IS	lu-	
defille	Table 6-10. E	rror and Thermal Protection Signals		ed V			
unc	Signal Name	Description	Dir.	Buffer Type	Link Type	Availability	1efineo
	CATERR#	Catastrophic Error: This signal indicates that the system has experienced a catastrophic error and cannot continue to operate. The processor will set this signal for non-recoverable machine check errors or other unrecoverable internal errors. CATERR# is used for signaling the following types of errors: Legacy MCERRs, CATERR# is asserted for 16 BCLKs. Legacy IERRs, CATERR# remains asserted until warm or cold reset.	0	OD	SE	All Processor Lines	UNOC
d undefined .	PECI	Platform Environment Control Interface: A serial sideband interface to the processor. It is used primarily for thermal, power, and error management. Details regarding the PECI electrical specifications, protocols and functions can be found in the RS-Platform Environment Control Interface (PECI) Specification, Revision 3.0.	I/O	PECI, Async	SE	All Processor Lines	undefined u
	PROCHOT#	Processor Hot: PROCHOT# goes active when the processor temperature monitoring sensor(s) detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. This signal can also be driven to the processor to activate the TCC.	I/O	GTL I OD O	SE	All Processor Lines	
ed undefined t	THERMTRIP#	Thermal Trip: The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all executions when the junction temperature exceeds approximately 130 °C. This is signaled to the system by the THERMTRIP# pin.	0	OD C	und SE	All Processor Lines	Indefined
	Datasheet, Volume 1	of 2 od undefin	e			undefine	1
d	unden.	undefine				Jefined -	
18fins		an ^{eo}			d 111		

(intel) red under

Table 6-11. Power Sequencing Signals

	undefine		defined			
intel) rea	stined	UIII		Signal Descriptio	nde
	Power Sequencing Sig	nals	5		ned une	
Table 6-11. Signal Name	Power Sequencing Signals Description	Dir.	Buffer Type	Link Type	Availability]
PROCPWRGD	Processor Power Good: The processor requires this input signal to be a clean indication that the V_{CC} and V_{DDQ} power supplies are stable and within specifications. This requirement applies regardless of the S-state of the processor. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal should then transition monotonically to a high state.	efine	CMOS	SE	All Processor Lines	undf
VCCST_PWRGD	VCCST Power Good: The processor requires this input signal to be a clean indication that the VCCST and VDDQ power supplies are stable and within specifications. This signal should have a valid level during both S0 and S3 power states. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal should then transition monotonically to a high state.	I Sefin	ed undefined cmos	SE	All Processor Lines	und
PROC_DETECT# /SKTOCC#	Processor Detect / Socket Occupied: Pulled down directly (0 Ohms) on the processor package to the ground. There is no connection to the processor silicon for this signal. System board designers may use this signal to determine if the processor is present.	N/A	N/A	SE	All Processor Lines	
VIDSOUT VIDSCK VIDALERT#	VIDSOUT, VIDSCK, VIDALERT#: These signals comprise a three-signal serial synchronous interface used to transfer power management information between the processor and the voltage regulator controllers.	I/O O I	I:GTL/O:OD OD CMOS	SE	All Processor Lines	d un
MSM#	Minimum Speed Mode: Control signal to VccEOPIO VR (connected only in 2 VR solution for OPC).	0	CMOS	SE	Processors w/ on- package cache	
ZVM#	Zero Voltage Mode: Control Signal to OPC VR, when low OPC VR output is 0V.	0	CMOS	SE	Processors w/ on- package cache	
ZVM#	ndefined undefined L.		ined undefine	d un		edu
ed undefined u	Zero Voltage Mode: Control Signal to OPC VR, when low OPC VR output is 0V.		Air-	ed un	defined undefin	
102	undefined une	unde	sined under		Datasheet, Volume 1 of	ned '
ned un-	ed unde			ل ال	ndefit	



red undefined undefined **Processor Power Rails**

Table 6-12. Processor Power Rails Signals

<section-header></section-header>	ined -	ed une				unter.
Signal Name Description Dir. Buffer Type Link Type Availability Vcc Processor IA cores power rail I Power – All Processor Lines Vccdu/1 Processor IA cores power rail I Power – All Processor Lines Vccdu/1 Processor Graphics power rail I Power – All Processor Lines Vccdu/1 Processor Graphics power rail I Power – All Processor Lines Vccdu/1 Processor Graphics power rail I Power – All Processor Lines Vccdu/1 Processor Graphics power rail I Power – All Processor Lines Vccau System Memory power rail Credits of Margon and Vccau power rail I Power – All Processor Lines Vccau Vccau Vccau Vccau II Power – All Processor Lines Vccau Processor VID power rails I Power – All Processor Lines Vccau Geted sustain voltage for processor standby modes I <th>6.8</th> <th>Processor Power Rails</th> <th></th> <th></th> <th>Jefin</th> <th></th>	6.8	Processor Power Rails			Jefin	
Signal NameDescriptionDirTypeTypeTypeAll Processor LinesVccProcessor IA cores pade power rail1Power-All Processor LineVccon1Processor IA cores gade power rail, connects to1Power-All Processor LineVccorProcessor Graphics power rail1Power-All Processor LinesVccorProcessor Graphics power rail1Power-All Processor LinesVccorSystem Memory power rail1Power-All Processor LinesVbogcSystem Memory power rail1Power-All Processor LinesVbogcSystem Memory cook power rail1Power-All Processor LinesVccsProcessor I/D power rail1Power-All Processor LinesVccgoProcessor I/D power rail1Power-All Processor LinesVccgoProcessor I/D power rail1Power-All Processor LinesVccgoProcessor I/D power rail1Power-All Processor LinesVccgoGeted sustain voltage for processor standby modes1Power-All Processor LinesVccgrdGeted sustain voltage for processor standby modes1Power-All Processor LinesVccgrdProcessor PLis power rails1Power-All Processor LinesVccgrdProcessor PC power rails1Power-All Processor LinesVccgrdProcessor PC power	Table 6-12.	Processor Power Rails Signals		20	no	
V _{CCG0/1} Processor IA cores gated power rail, connects to 1 Power - V/Processor Lines IIII VCCGrt Processor Graphics power rail 1 Power - All Processor Lines VCCGrtx Processor Graphics power rail (extension) 1 Power - All Processor Lines Vpogc System Memory power rail 1 Power - All Processor Lines Vpogc through IP fitter. 1 Power - All Processor Lines VcCig Processor System Agent power rail 1 Power - All Processor Lines VcCig Processor Jupes Agent power rail 1 Power - All Processor Lines VcCig Processor Plate power rails 1 Power - All Processor Lines VcCig Gated sustain voltage for processor standby modes 1 Power - All Processor Lines VcCquL Processor PLLS power rails 1 Power - All Processor Lines VcCquC Processor OPC power rails 1 Power	Signal Nam	e Description	Dir.			Availability
VCC00/1 board capacitors for filtering. I Power - AML/Y22 Processor Line VCCGT Processor Graphics power rail I Power - All Processor Lines VCCGTX Processor Graphics power rail I Power - All Processor Lines VDog System Memory clock power rail I Power - All Processor Lines VDogc System Memory clock power rail I Power - All Processor Lines VCcgo System Memory clock power rail I Power - All Processor Lines VCcgo VCcgo power rail. Consists of VCc10 and VCcgo pow. VCc1 and VCc10 power rails I Power - All Processor Lines VCcgrs Gated sustain voltage for processor standby modes I Power - All Processor Lines VCcgrt1_0 Processor PLLs power rails I Power - All Processor Lines VCcqu Processor OPC power rails I Power - All Processor Lines VCcqrt2_1pa Processor OPC power rails I Power - All Processor Lines VCcqL_1oc <td>Vcc</td> <td>Processor IA cores power rail</td> <td>I</td> <td>Power</td> <td>—</td> <td>All Processor Lines</td>	Vcc	Processor IA cores power rail	I	Power	—	All Processor Lines
VCGTX Processor Graphics power rail (extension) I Power Processor W GT3 VDoQ System Memory power rail I Power - All Processor Lines VDoQC through JP fitter I Power - All Processor Lines VCCga Processor System Agent power rail I Power - All Processor Lines VCCga Processor J/O power rail. Consists of V _{CCID} and V _{CCTO DBR} should be isolated I Power - All Processor Lines VCCga Processor J/O power rails I Power - All Processor Lines VCCga Gated sustain voltage for processor standby modes I Power - All Processor Lines VCcgrL Processor PLLs power rails I Power - All Processor Lines VCcpLL_OC Processor OPC power rails I Power - All Processor W orn- VCcpc_L_DC Processor OPC power rails I Power - All Processor W orn- VCcgrL_DC Processor OPC power rails I Power <t< td=""><td>V_{CCG0/1}</td><td></td><td>I</td><td>Power</td><td>_</td><td>AML-Y22 Processor</td></t<>	V _{CCG0/1}		I	Power	_	AML-Y22 Processor
Vision System Memory power rail I Power All Processor Lines Vision System Memory clock power rail, feeds from VDDQ I Power All Processor Lines Vicity Processor System Agent power rail 1 Power All Processor Lines Vicity Processor System Agent power rail 1 Power All Processor Lines Vicity Processor System Agent power rail 1 Power All Processor Lines Vicity Sustain voltage for processor standby modes 1 Power All Processor Lines Vicity Gated sustain voltage for processor standby modes 1 Power All Processor Lines Vicity Gated sustain voltage for processor standby modes 1 Power All Processor Lines Vicity Processor PLLs power rails 1 Power All Processor W/O Vicept_L Processor OPC power rails 1 Power All Processor W/O Vicept_Loc Processor OPC power rails 1 Power - All Processor W/O Vicept_Loc Processor OPC power rails 1 Power - All Processor W/O Vicept_Sense Isolate	Vcc _{GT}	Processor Graphics power rail	I	Power	_	All Processor Lines
Und System Memory clock power rail, feeds from VDDQ 1 Power - U/Y-Processor Lines AML-Y22 Processor AML-Y22 Processor Lines VCc _{SA} Processor System Agent power rail 1 Power - All Processor Lines VCc _{SA} Processor System Agent power rail 1 Power - All Processor Lines VCc _{ST} System March VCciro park dubt be isolated 1 Power - All Processor Lines VCc _{ST} System March VCciro park dubt be isolated 1 Power - All Processor Lines VCc _{ST} System VCciro and VCciro park dubt be isolated 1 Power - All Processor Lines VCc _{STO} System VCciro and VCciro park dubt be isolated 1 Power - All Processor Lines VCc _{STO} System VCciro and VCciro park dubt be isolated 1 Power - All Processor Lines VCc _{STO} Gated sustain voltage for processor standby modes 1 Power - All Processor Lines VCc _{PLL} Processor PLLs power rails 1 Power - All Processor Lines VCc _{PLL} oc Processor OPC power rails 1 Power - Processors w/ on-package cache Vcc _{OPC} and Processor OPC power rails 1 Power </td <td>Vcc_{GTX}</td> <td>Processor Graphics power rail (extension)</td> <td>I</td> <td>Power</td> <td>-</td> <td>Processors w/ GT3</td>	Vcc _{GTX}	Processor Graphics power rail (extension)	I	Power	-	Processors w/ GT3
VDDQC through LP filter. I Power - AML-Y22 Processor Une VCcSA Processor I/O power rail. Consists of V _{CCQ} and VCcG0 VCcG0, DOP. V _{CCQ} and VCC0_DDR should be isolated from each other. I Power - All Processor Lines VCcG1 VCcS3T Sustain voltage for processor standby modes I Power - All Processor Lines VCcS3T Gated sustain voltage for processor standby modes I Power - All Processor Lines VCcS3T Gated sustain voltage for processor standby modes I Power - All Processor Lines VCcS1C Gated sustain voltage for processor standby modes I Power - All Processor Lines VCcD1L_OC Processor PLLs power rails I Power - All Processor VIC VCcD0C Processor OCP power rails I Power - All Processor VIC VCcD0C Processor OCP power rails I Power - All Processor VIC VCcD0C Processor OCP power rails I Power - All Processor VIC VCcG0C Processor OCP power rails I Pow	V _{DDQ}	System Memory power rail	Ι	Power	781	All Processor Lines
Vcc ₁₀ Processor I/0 power rail. Consists of V _{CC10} and Vcc ₁₀ pok. Vccno and V _{CC10} pok should be isolated I Power – All Processor Lines Vcc ₁₀ Sustain voltage for processor standby modes I Power – All Processor Lines Vcc _{5TG} Sustain voltage for processor standby modes I Power – All Processor Lines Vcc _{5TG} Gated sustain voltage for processor standby modes I Power – All Processor Lines Vcc _{9LL} Processor PLLs power rails I Power – All Processor Lines Vcc _{0PC} Processor OPC power rails I Power – All Processor Vice Vccopc_lp8 Processor OPC power rails I Power - Processors w/ on- package cache Vcc _{0PC_lp8} Processor OPC power rails I Power - Processor w/ on- package cache Vcc _{10D} SENSE Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - All Processor Lines Vcc _{0DC_SENSE} Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - <td>V_{DDQC}</td> <td></td> <td>I</td> <td>Power</td> <td>un<u>-</u></td> <td>AML-Y22 Processor</td>	V _{DDQC}		I	Power	un <u>-</u>	AML-Y22 Processor
VCcto VCcto DDB VCcto DDB VCcto DDB VCcST Sustain voltage for processor standby modes I Power - All Processor Lines VCcSTG Gated sustain voltage for processor standby modes I Power - All Processor Lines VCcSTG Gated sustain voltage for processor standby modes I Power - All Processor Lines VCcGL Processor PLLS power rails I Power - All Processor Lines VCcPLL_OC Processor PLS power rails I Power - All Processor Vines VCcOPC_Lp8 Processor OPC power rails I Power - Processors Vin-package cache VCcOPC_Lp8 Processor OPC power rails I Power - Processors Vin-package cache Vcc_SENSE Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - All Processor Lines VccGIT_SENSE Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - All Processor Lines VccGIT_SENSE Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - All Processor Lin	Vcc _{SA}	Processor System Agent power rail	I	Power	—	All Processor Lines
Vcc _{STG} Gated sustain voltage for processor standby modes I Power KBL U/Y-Processor Lines Vcc _{PLL} Processor PLLs power rails I Power – All Processor Lines Vcc _{PLL} _OC Processor PLLs power rails I Power – All Processor Lines Vcc _{PLL} _OC Processor OPC power rails I Power – All Processor SW (on- package cache Vcc _{OPC_1D8} Processor OPC power rails I Power - Processors W (on- package cache Vcc _{OPC_1D8} Processor OPC power rails I Power - Processors W (on- package cache Vcc _{OPC_1D8} Processor OPC power rails I Power - Processors W (on- package cache Vcc _{OPC_1D8} Processor OPC power rails I Power - Processors W (on- package cache Vcc _{DPC_1D8} Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - All Processor Lines Vcc _{GT_SENSE} Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - All Processor Lines V	Vcc _{IO}	Vcc _{IO DDR} . V _{CCIO} and V _{CCIO DDR} should be isolated	I	Power	_	All Processor Lines
VCc _{STG} I Power Lines' AML-Y22 Processor Lines VCc _{PLL} Processor PLLs power rails I Power All Processor Lines VCc _{PLL} OC Processor PLLs power rails I Power All Processor Lines Vcc _{OPC} Processor OPC power rails I Power All Processor W on- package cache Vcc _{OPC_1P8} Processor OPC power rails I Power - Processors W on- package cache Vcc _{OPC_1P8} Processor OPC power rails I Power - Processors W on- package cache Vcc _{OPC_1P8} Processor OPC power rails I Power - Processors W on- package cache Vcc _{OPC_1P8} Processor OPC power rails I Power - All Processor Lines Vcc _{OPC_1P8} Isolated, low impedance voltage sense pins. They vss_SENSE Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - All Processor Lines Vcc _{GT_SENSE} Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the vss_GS_SENSE N/A Power - All Processor Lines	Vcc _{ST}	Sustain voltage for processor standby modes	I	Power	-	All Processor Lines
VCcpLL_OC Processor PLLs power rails I Power All Processor Lines VCcQpC Processor OPC power rails I Power Processor W on-package cache VCcOPC_1p8 Processor OPC power rails I Power Processors W on-package cache VCcOPC_1p8 Processor OPC power rails I Power Processors W on-package cache VCc_OPIO Processor OPC power rails I Power Processors W on-package cache VCc_SENSE Isolated, low impedance voltage sense pins. They Processor Lines N/A Vss_SENSE Isolated, low impedance voltage sense pins. They N/A Power All Processor Lines VccGTX_SENSE Isolated, low impedance voltage sense pins. They N/A Power All Processor W GT3 VccGTX_SENSE Isolated, low impedance voltage sense pins. They N/A Power Processor W GT3 VccGTX_SENSE Isolated, low impedance voltage sense pins. They N/A Power Processor W GT3 VccGTX_SENSE Isolated, low impedance voltage sense pins. They N/A Power Processor W GT3 VccGTX_SENSE Isolated, low impedance voltage sense pins. They N/A Pow	Vcc _{STG}	Gated sustain voltage for processor standby modes	I	Power	-	Lines AML-Y22 Processor
VCCOPC Processor OPC power rails I Power - Processors w/ on-package cache VCCOPC_1p8 Processor OPC power rails I Power - Processors w/ on-package cache VCCOPC_1p8 Processor OPC power rails I Power - Processors w/ on-package cache VCCOPC_1p8 Processor OPC power rails I Power - Processors w/ on-package cache VCCOPC_SENSE Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - All Processor Lines VCcGT_SENSE Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - All Processor w/ GT3 VccGT_SENSE Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - All Processor w/ GT3 VccGGT_SENSE Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - All Processor Lines VccGGT_SENSE Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - All Processor Lines<	Vcc _{PLL}	Processor PLLs power rails	Ι	Power	JA	All Processor Lines
VCCopc I Power - package cache VCCopc_1p8 Processor OPC power rails I Power - Processors w/ on-package cache VCc_EOPID Processor OPC power rails I Power - Processors w/ on-package cache Vcc_SENSE Isolated, low impedance voltage sense pins. They I Power - All Processor Lines Vcc_GT_SENSE Isolated, low impedance voltage sense pins. They N/A Power - All Processor Lines VccGT_SENSE Isolated, low impedance voltage sense pins. They N/A Power - All Processor Lines VccGT_SENSE Isolated, low impedance voltage sense pins. They N/A Power - All Processor w/ GT3 VccGT_SENSE Isolated, low impedance voltage sense pins. They N/A Power - All Processor w/ GT3 VccGT_SENSE Isolated, low impedance voltage sense pins. They N/A Power - All Processor w/ GT3 VccGT_SENSE Isolated, low impedance voltage sense pins. They N/A Power - All Processor Lines VccGT_SENSE Isolated, low impedance voltage sense pins. They N/A	Vcc _{PLL_OC}	Processor PLLs power rails	I	Power	_	All Processor Lines
Vcc _{OPC_1p8} Processor OPC power rails I Power - Processors w/ on-package cache Vcc _{OPC_1p8} Processor OPC power rails I Power - Processors w/ on-package cache Vcc_SENSE Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - All Processor W/ on-package cache Vcc_ST_SENSE Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - All Processor w/ GT3 VccGTX_SENSE Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - All Processor w/ GT3 VccGTX_SENSE Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - All Processor w/ GT3 Vccs_SINSE Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - All Processor Lines Vccs_SINSE Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - All Processor Lines Vccs_SINSE Isolated, low impedance voltage sen	Vcc _{OPC}	Processor OPC power rails	I	Power	-	
VCCCOPTO Image: Ima	Vcc _{OPC_1p8}	Processor OPC power rails	с I	Power	-	Processors w/ on-
Vcc_sLNSL can be used to sense or measure voltage near the silicon. N/A Power - All Processor Lines VcccgT_SENSE Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - All Processor Lines VccgT_SENSE Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - All Processor Lines VccgT_SENSE Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - All Processor W GT3 Vccto_SENSE Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - All Processor Lines Vccto_SENSE Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - All Processor Lines Vccs_SENSE Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - All Processor Lines Vccs_SENSE Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - All Processor W on-package cache	Vcc _{EOPIO}	Processor OPC power rails	I	Power	-	
VcGgT_SENSE can be used to sense or measure voltage near the silicon. N/A Power - All Processor Lines VcGgTx_SENSE Isolated, low impedance voltage sense pins. They used to sense or measure voltage near the silicon. N/A Power - Processors w/ GT3 VccgTx_SENSE Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - All Processor Lines Vccg_SENSE Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - All Processor Lines Vccs_SA_SENSE Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - All Processor Lines Vccs_SA_SENSE Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - All Processor Lines Vccopc_SENSE Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - All Processor Lines Vcscopc_SENSE Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - Processors w/ on-package cache		can be used to sense or measure voltage near the	N/A	Power	-	All Processor Lines
VccGTX_SENSE can be used to sense or measure voltage near the silicon. N/A Power - Processors w/ GT3 Vcc10_SENSE Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - All Processor Lines Vcc5A_SENSE Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - All Processor Lines VccSA_SENSE Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - All Processor Lines VccOPC_SENSE Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - All Processor Lines VcCoPC_SENSE Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - Processors w/ on-package cache VccEOPIO_SENSE Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - Processors w/ on-package cache VsEOPIO_SENSE Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - Processors		can be used to sense or measure voltage near the	N/A	Power	d undi	All Processor Lines
Vcc10_StNSE can be used to sense or measure voltage near the silicon. N/A Power - All Processor Lines Vcc5A_SENSE Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - All Processor Lines Vcc0PC_SENSE Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - All Processor Lines Vcc0PC_SENSE Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - Processors w/ on-package cache VccEOPIO_SENSE Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - Processors w/ on-package cache VcsEOPIO_SENSE Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - Processors w/ on-package cache VssEOPIO_SENSE Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - Processors w/ on-package cache Datasheet, Volume 1 of 2 Datasheet in figure 1 1 1		can be used to sense or measure voltage near the	N/A	Power	-	Processors w/ GT3
Viciga_JENSE can be used to sense or measure voltage near the silicon. N/A Power - All Processor Lines Viciga_SENSE Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - Processors w/ on-package cache Viciga_SENSE Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - Processors w/ on-package cache Vice_EOPIO_SENSE Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - Processors w/ on-package cache Vastering Sense Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - Processors w/ on-package cache Vastering Sense Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - Processors w/ on-package cache Datasheet, Volume 1 of 2 Isolated Isolated Isolated Isolated Isolated Isolated		can be used to sense or measure voltage near the	N/A	Power	-	All Processor Lines
Victopestivit can be used to sense or measure voltage near the silicon. N/A Power - Processors W/ on-package cache Vcce_OPIO_SENSE Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - Processors w/ on-package cache Vcce_OPIO_SENSE Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon. N/A Power - Processors w/ on-package cache Datasheet, Volume 1 of 2 Datasheet, Volume 1 of 2 10		can be used to sense or measure voltage near the	N/A	Power	_	All Processor Lines
Datasheet, Volume 1 of 2		can be used to sense or measure voltage near the	N/A	Power	. und	package cache
Datasheet, Volume 1 of 2		can be used to sense or measure voltage near the	N/A	Power	30 <u>-</u>	Processors w/ on- package cache
		ndefined undefined undefined	hed u			defined undefin

intel red under

6.9

Ground, Reserved and Non-Critical to Function (NCTF) Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

- RSVD these signals should not be connected
- RSVD_TP these signals should be routed to a test point
- RSVD_NCTF these signals are non-critical to function and may be left unconnected

Arbitrary connection of these signals to VCC, VDDQ, VSS, or to any other signal (including each other) may result in component malfunction or incompatibility with future processors. See Table 6-13, "GND, RSVD, and NCTF Signals".

For reliable operation, always connect unused inputs or bi-directional signals to an appropriate signal level. Unused active high inputs should be connected through a resistor to ground (V_{SS}). Unused outputs may be left unconnected however, this may interfere with some Test Access Port (TAP) functions, complicate debug probing and prevent boundary scan testing. A resistor should be used when tying bi-directional signals to power or ground. When tying any signal to power or ground, the resistor can also be used for system testability.

Table 6-13. GND, RSVD, and NCTF Signals

Signal Name	Description
Vss	Processor ground node
Vss_NCTF	Non-Critical To Function: These signals are for package mechanical reliability.
RSVD	Reserved : All signals that are RSVD should not be connected on the board.
RSVD_NCTF	RSVD_NCTF : RSVD_NCTF should not be connected on the board.
RSVD_TP	RSVD_TP : Intel recommends to route each RSVD_TP to an accessible test point. Intel may require these test points for platform specific debug. Leaving these test points inaccessible could delay debug by Intel.

undefined undefined un Processor Internal Pull-Up / Pull-Down Terminations

Table 6-14. Processor Internal Pull-Up / Pull-Down Terminations

undefine 6.10	Processor In Terminations	ternal Pull-Up /	Pull-Down	1	. red u
Table 6	-14. Processor Internal I	Pull-Up / Pull-Down Term	inations		ndefit
	Signal Name	Pull Up/Pull Down	Rail	Value	ed un
	BPM[3:0]	Pull Up / Pull Down	Vcc _{IO}	16-60 ohms	
275	PREQ#	Pull Up	Vcc _{ST}	3 kohms	
undefined undefin	PROC_TDI	Pull Up	Vcc _{STG}	3 kohms	
d un	PROC_TMS	Pull Up	Vcc _{STG}	3 kohms	
sinec	PROC_TRSN#	Pull Down	- <u>,</u> un	3 kohms	
der	CFG[19:0]	Pull Up	Vcc _{IO}	3 kohms	.6-
ed t	red undefined unc	defined	unden		ined undefine
104	nedt	undefined une	I	Datasheet, Volume 1 c	of 2
retines	2.55	led .	d ul		





Electrical Specifications

7.1 **Processor Power Rails**

	-				
		defined	sined un		ed und
	7.1	Processor Power Rails	S under	A UT	define
	Table 7-1.	Processor Power Rails	Still.	efiner	
	Power Rail	Description	Control	Availability	
2	V _{cc}	Processor IA Cores Power Rail	SVID	All Processor Lines	
, une	Vcc _{GT}	Processor Graphics Power Rails	SVID	All Processor Lines	
	Vcc _{GTX} Note 2,6	Processor Graphics Extended Power Rail	SVID	Processors w/ GT3	
efili	Vcc _{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)	All Processor Lines	710
	Vcc _{IO}	IO Power Rail	Fixed	All Processor Lines	
	Vcc _{ST}	Sustain Power Rail	Fixed	All Processor Lines	stine
	Vcc _{STG} ⁵	Sustain Gated Power Rail	Fixed	U/Y-Processor Lines AML-Y22 Processor Line	
	Vcc _{PLL}	Processor PLLs power Rail	Fixed	All Processor Lines	
	Vcc _{PLL_OC} 4	Processor PLLs OC power Rail	Fixed	All Processor Lines	
	V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)	All Processor Lines	
d un	Vcc _{OPC} ³	Processor OPC power Rail	Fixed	Processors w/OPC	
	Vcc _{OPC_1P8} ³	Processor OPC power Rail	Fixed	Processors w/OPC	
9e	Vcc _{EOPIO} ³	Processor EOPIO power Rail	Fixed	Processors w/OPC	y ur
	Notes: 1. N/A	innacted for Processors without CT2	ndefini		1efineo

Table 7-1. **Processor Power Rails**

2. Rail is unconnected for Processors without GT3.

3. Rail is unconnected for Processors without OPC.

VCc_{PLL_OC} power rail should be sourced from the VDDQ VR. The connection can be direct or through a load switch, depending desired power optimization. In case of direct connection (Vcc_{PLL_OC} is shorted to V_{DDQ} , no load switch), platform 4. should ensure that Vcc_{STG} is ON (high) while Vc_{PLL_OC} is ON (high). Vcc_{STG} power rail should be sourced from the VR as V_{CCST} . The connection can be direct or through a load switch, 5.

depending desired power optimization.

6. Intel has added the option of merging the GT/GTx power rails for the U-Processor Line GT3 product family.

7.1.1 **Power and Ground Pins**

All power pins should be connected to their respective processor power planes, while all VSS pins should be connected to the system ground plane. Use of multiple power and ground planes is recommended to reduce I*R drop.

7.1.2

V_{CC} Voltage Identification (VID)

Intel processors/chipsets are individually calibrated in the factory to operate on a specific voltage/frequency and operating-condition curve specified for that individual processor. In normal operation, the processor autonomously issues voltage control requests according to this calibrated curve using the serial voltage-identifier (SVID) red undefiner interface. Altering the voltage applied at the processor/chipset causing operation outside of this calibrated curve is considered out-of-specification operation. The SVID bus consists of three open-drain signals: clock, data, and alert# to both set

Electrical Specifications



7.2

voltage-levels and gather telemetry data from the voltage regulators. Voltages are controlled per an 8-bit integer value, called a VID, that maps to an analog voltage level. red undefined und An offset field also exists that allows altering the VID table. Alert can be used to inform the processor that a voltage-change request has been completed or to interrupt the processor with a fault notification.

DC Specifications

The processor DC specifications in this section are defined at the processor signal pins, unless noted otherwise.

- The DC specifications for the DDR3L/-RS/LPDDR3/DDR4 signals are listed in the Voltage and Current Specifications section.
- The Voltage and Current Specifications section lists the DC specifications for the processor and are valid only while meeting specifications for junction temperature, clock frequency, and input voltages. Read all notes associated with each parameter.
- AC tolerances for all DC rails include dynamic load currents at switching frequencies up to 1 MHz.

Processor Power Rails DC Specifications 7.2.1

7.2.1.1 Vcc DC Specifications

Table 7-2. Processor IA core (Vcc) Active and Idle Mode DC Voltage and Current Specifications (Sheet 1 of 3)

Ī	Symbol	Parameter	Segment	Min	Turn	Max	Unit	Note ¹	1
	Symbol	and the second sec	Segment	MILLI	Тур	Мах	Unit		_
	Operating Voltage	Voltage Range for Processor Operating Modes	All		9ezin	1.52	ev Vev	1, 2, 3, 7, 12	
		cineo.	Y-Processor Line (4.5W)	<u> </u>	-	24			
	und	e),	Y-Processor Line (6W) Pentium/Celeron	_	_	24			
	. red		AML-Y22 Processor Line (5W)	-	—	28			
inde	ined und		U-Processor Line (15W) - 2 Core GT2,GT1	_	_	32			0
	Icc _{MAX} (U/Y- Processors)	Maximum Processor IA Core I _{CC}	U-Processor Line (15W) - 2 Core GT1 Pentium/Celeron	_	-	ed under 29	A	4, 6, 7, 11	
	,	d unde	U-Processor Line (15W) - 4 Core GT2 (U- 4 Core)	_	19et	64	Inec		
		Jefines	U-Processor Line (15W) - 2 Core GT3+OPC	eq.	_	32 woed une			
	med un		U-Processor Line (28W) - 2 Core GT3+OPC	_	_	32 100			
26			sines			ed			
, une	TOB _{VCC}	Voltage Tolerance	PS0, PS1	-	—	±20	mV	3, 6, 8	le
,O	ισυγίι		PS2, PS3	-		±20		5, 0, 0	
		ndefined undefi	nec undefi		26	ined L	eined	unc	
	106			1	JUC.	Datasheet, Volume 1	of 2		
		1 efilt				-d un			
						Aines			
	ed u		4 Une						
	elilie					du			

led underine **Electrical Specifications**



	Parameter	Segment	Min	Тур	14	Max		Unit	Not
		10110	1	1	I _L <=0.5 0.5<	IL <icctdc< th=""><th>Icc_{TDC}<il<icc<sub>MAX</il<icc<sub></th><th></th><th>-</th></icctdc<>	Icc _{TDC} <il<icc<sub>MAX</il<icc<sub>		-
	_1	PS0	-	_	+30/-10	±10	±15	-	ine
Ripple	Ripple Tolerance	PS1	_		+30/-10	±15	±15	mV	3, 6
	stine	PS2	-	20		30/-10	+30/-10	U	
	inde	PS3	20	- 1		30/-10	+30/-10	1	
	d'	Y-Processor Line	- 1	_		5.9	der.		
		AML-Y22 Processor Line (5W)	-	_		4	4 un		
DC_LL (U/Y-	Loadline slope within the VR regulation	U-Processor Line - 2 Core GT2,GT1	-	_		2.4	100	mΩ	10,
Processors)	loop capability	U-Processor Line (U-4 Core) - 4-Core			ined	2.4		11152	1
	6	U-Processor Line - 2 Core GT3 with OPC			Indern	2.4		6	etin
AC_LL (Y/U- Processors)	AC Loadline	U-Processor Lines	20	iner (Same as f	Max DC_LL	(up to 1MHz)	mΩ	10, 1
AC_LL (Y- Processors)	AC Loadline	AML-Y22-Processor Line	- 100	_	(frequency) • 2MHz – 20N	from 4 to 1Hz: 6 MHz: Incre ncy) from 6	asing linearly with	mΩ	10, 14,
AC_LL (Y- Processors)	AC Loadline	Y-Processor Line	-	-	(frequency) • 4MHz – 20M	z:Increasin from 5.9 to Hz: 11.7 MHz: Increa cy) from 11	asing linearly with	mΩ	10, 14
T_OVS_TD P_MAX	Max Overshoot time TDP/virus mode	-	Uno	-		10/30	, unden.	μs	
V_OVS TDP_MAX/ virus_MAX	Max Overshoot at TDP/virus mode	- undefine	-	_		70/200	tineo	mV	
<u>e</u>	L								
	sined undefine	d undefine	d un	Jefin	ed undefine	,d un	undefit	ned ut	ndef
ned und	stined undefine	d undefined undefine	d un	Jetin	ed undefine	ed und	afined undefin	ned un	Indef
ned undf	isheet, Volume 1 of 2	d undefine	d un	Jefin	ed undefine	ed und	afined undefin	ned ur ined u	Inde
ned und Data	isheet, Volume 1 of 2	d undefined undefine	ed un	Jefin	ed undefine	ed und	efined undefin	ned un 107	Inde

ed undefined undefined ndefined Processor IA core (Vcc) Active and Idle Mode DC Voltage and Current Table 7-2.



ed undefined undefined Processor IA core (Vcc) Active and Idle Mode DC Voltage and Current Specifications (Sheet 3 of 3)

	d'u		cations (Sheet 3 of 3	-		nde'		
	Syn	nbol Parameter	Segment	Min	Тур	Max	Unit	Note ¹
	Notes	s:	1elli			inot		-0
					ates and	simulations or empirical data. These	se specifications will be	e updated
		with characterized data from sili						
						VID) that is set at manufacturing a		
						s at the same frequency may have		
				ocessor dur	ing a pov	ver management event (Adaptive T	Thermal Monitor, Enha	nced Intel
		SpeedStep Technology, or low-p					24	
	З. Т	i ne voltade specification reduire	ments are measured across v	CC_SENSE a	ina vss_s	SENSE as near as possible to the pr	ocessor with an oscilic	oscope set
				and 1 MO m	1	was a damage. The a second second law adda a	. مماط منه مترانين استنتخبت ع	
	t	to 100-MHz bandwidth, 1.5 pF n	naximum probe capacitance,			mpedance. The maximum length o	of ground wire on the p	
	t	to 100-MHz bandwidth, 1.5 pF n should be less than 5 mm. Ensu	naximum probe capacitance, re external noise from the sys	stem is not o			of ground wire on the p	
	t s 4. F	to 100-MHz bandwidth, 1.5 pF n should be less than 5 mm. Ensu Processor IA core VR to be desig	naximum probe capacitance, re external noise from the sys aned to electrically support th	stem is not o is current.	coupled i	nto the oscilloscope probe.	of ground wire on the p	
	t 9 4. F 5. F	to 100-MHz bandwidth, 1.5 pF n should be less than 5 mm. Ensu Processor IA core VR to be desig Processor IA core VR to be desig	naximum probe capacitance, re external noise from the sys gned to electrically support the gned to thermally support this	stem is not o is current. s current ind	coupled i efinitely.	nto the oscilloscope probe.	of ground wire on the p	
	t 4. F 5. F 6. L	o 100-MHz bandwidth, 1.5 pF n should be less than 5 mm. Ensu Processor IA core VR to be desio Processor IA core VR to be desio Long term reliability cannot be a	naximum probe capacitance, re external noise from the sy gned to electrically support th gned to thermally support this issured if tolerance, ripple, ar	stem is not on is current. s current ind nd core noise	coupled i efinitely. e parame	nto the oscilloscope probe.	of ground wire on the p	
	t 4. F 5. F 6. L 7. L	to 100-MHz bandwidth, 1.5 pF n should be less than 5 mm. Ensu Processor IA core VR to be desic Processor IA core VR to be desic ong term reliability cannot be a Long term reliability cannot be a	naximum probe capacitance, re external noise from the sy- gned to electrically support thi gned to thermally support this issured if tolerance, ripple, ar assured in conditions above or	stem is not of is current. s current ind nd core noise r below Max,	coupled i efinitely. e parame /Min func	nto the oscilloscope probe.	f ground wire on the p	
	t 4. F 5. F 6. L 7. L 8. F	to 100-MHz bandwidth, 1.5 pF n should be less than 5 mm. Ensu Processor IA core VR to be desig processor IA core VR to be desig ong term reliability cannot be a song term reliability cannot be a PSx refers to the voltage regular	naximum probe capacitance, re external noise from the sy- gned to electrically support thi gned to thermally support this issured if tolerance, ripple, ar assured in conditions above or	stem is not of is current. s current ind nd core noise r below Max,	coupled i efinitely. e parame /Min func	nto the oscilloscope probe.	f ground wire on the p	
Jefir	t 4. F 5. F 6. L 7. L 8. F 9. N	to 100-MHz bandwidth, 1.5 pF n should be less than 5 mm. Ensu Processor IA core VR to be desig Processor IA core VR to be desig Long term reliability cannot be a Sx refers to the voltage regular V/A	naximum probe capacitance, re external noise from the sy- gned to electrically support thi gned to thermally support this issured if tolerance, ripple, ar assured in conditions above or	stem is not of is current. s current ind nd core noise r below Max,	coupled i efinitely. e parame /Min func	nto the oscilloscope probe.	f ground wire on the p	
Jefir	t 4. F 5. F 6. L 7. L 8. F 9. N 10. L	to 100-MHz bandwidth, 1.5 pF n should be less than 5 mm. Ensu Processor IA core VR to be desig Processor IA core VR to be desig long term reliability cannot be a ong term reliability cannot be a PSx refers to the voltage regular V/A L measured at sense points.	naximum probe capacitance, re external noise from the sy- gned to electrically support th gned to thermally support this assured if tolerance, ripple, ar assured in conditions above or tor power state as set by the	stem is not o is current. s current ind nd core noise r below Max, SVID protoc	coupled i efinitely. e parame /Min func col.	nto the oscilloscope probe. eters are violated. ctional limits.	une	probe
Jefir	t 4. F 5. F 6. L 7. L 8. F 9. N 10. L 11. T	to 100-MHz bandwidth, 1.5 pF n should be less than 5 mm. Ensu Processor IA core VR to be desig Processor IA core VR to be desig long term reliability cannot be a ong term reliability cannot be a PSx refers to the voltage regular V/A L measured at sense points.	naximum probe capacitance, re external noise from the sy- gned to electrically support the insured if tolerance, ripple, ar assured in conditions above or tor power state as set by the or commercial application it is	stem is not o is current. s current ind nd core noise r below Max, SVID protoc	coupled i efinitely. e parame /Min func col.	nto the oscilloscope probe.	une	probe
efil	4. F 5. F 6. L 7. L 8. F 9. N 10. L 11. T	to 100-MHz bandwidth, 1.5 pF n should be less than 5 mm. Ensu Processor IA core VR to be desig rocessor IA core VR to be desig ong term reliability cannot be a long term reliability cannot be a Sx refers to the voltage regular V/A L measured at sense points. Typ column represents Icc _{MAX} for	naximum probe capacitance, re external noise from the sy- gned to electrically support the gned to thermally support this issured if tolerance, ripple, ar assured in conditions above of tor power state as set by the or commercial application it is ed.	stem is not o is current. s current ind nd core noise r below Max, SVID protoc	coupled i efinitely. e parame /Min func col.	nto the oscilloscope probe. eters are violated. ctional limits.	une	probe
efil	4. F 5. F 6. L 7. L 8. F 9. N 10. L 11. T 12. 0	to 100-MHz bandwidth, 1.5 pF n should be less than 5 mm. Ensu Processor IA core VR to be desig ong term reliability cannot be a Sx refers to the voltage regular V/A L measured at sense points. Typ column represents Icc _{MAX} fo penchmarks that can be exceed Operating voltage range in stead	naximum probe capacitance, re external noise from the sy- ned to electrically support the gned to thermally support this support the system issured if tolerance, ripple, ar issured in conditions above or tor power state as set by the or commercial application it is ed. dy state.	stem is not of is current. s current ind nd core noise r below Max, SVID protoc NOT a spec	coupled i lefinitely. e parame /Min func col. ification	nto the oscilloscope probe. eters are violated. ctional limits.	samples using limited	probe

Line BIOS programming directly affects operating voltages (AC) and power measurements (DC). A superior board design with a shallower AC Load Line can improve on power, performance, and thermals compared to boards designed for POR impedance.
 15. For more details on AML-Y22 loadline target, refer to Power Integrity Model Set Doc ID# 597383.

7.2.1.2 Vcc_{GT} and Vcc_{GTX} DC Specifications

Processor Graphics (Vcc_{GT}and Vcc_{GTX}) Supply DC Voltage and Current Specifications (Sheet 1 of 2) Table 7-3.

2	7.2.1.2	Vcc _{G1}	_r and Vcc _{GTX} DC Sp	ecifi	catior	is defined t			
indefined	Table 7-3	3. Proce Specif	ssor Graphics (VCC _{GT} fications (Sheet 1 of	r <mark>and</mark> 2)	Vcc _G	TX) Supply DC Voltage and Current	-		ed un
0.	Symbol	Parameter	Segment	Min	Тур	Max	Unit	Note ¹	ine
	Operating voltage	Active voltage Range for Vcc _{GT}	All	0	-	1.52	ved	2,3,6, 8	
-	2	9	Y-Processor Line (4.5W)	—		24	÷		
	indefine		AML-Y22- Processor Line (5W)	tite ^e	-	24 sined un			
undefined	U.	Content for Content for Craphics	Y-Processor Line (6W) Pentium/Celeron	—	-	24			
under.	Icc _{MAX_GT} / Icc _{MAX_GTx} (U/Y- Processors)		U-Processor Line (15W) - 2 Core GT2,GT1	_	-	actine 31	A	6	ined u
5			U-Processor Line (15W) - 4 Core GT2 (U-4 Core)	_	-	od under 31		und	311
			U-Processor Line (15W) - 2 Core GT1 Pentium/Celeron	_	uni	etine 31	tine	0	
			U-Processor Line (15,28W)- 2 Core GT3 with OPC	8 <u>4</u> 108	_	Merged: 64(GT+GTx) Separate: GT-57/GTx-19		6,11, 12	
sine	TOB _{GT}	Vcc _{GT}	PS0,PS1	-	—	±20	mV	3, 4	
dell		Tolerance	PS2,PS3	-	-	±20	mV	3, 4	2
ed un		hed undef	Ined unde			Datasheet, Volume		ed und	Jefined 1
	108	hed un.			ed un	Datasheet, Volume	1 of 2		
	d under.		d un	defin		indefineo			
16111			sineu			d ^u			



Jun.	Symbol	Parameter	Segment	Min	Тур		Max		Unit	Note
			Yeun -			I _L <=0.5	0.5 <il<icc<sub>TDC</il<icc<sub>	$Icc_{TDC} < I_{L} < Icc_{MAX}$		
			PSO	—	—	+30/-10	±10	±15		117
	Ripple	Ripple Tolerance	PS1	-	—	+30/-10	±15	±15	mV	3,4
		16111	PS2	—	0.5	+30/-10	+30/-10	+30/-10		
		10	PS3	-	9e, .	+30/-10	+30/-10	+30/-10		
DC_LL (UY- Proces	ed		Y/AML-Y22 -Processor Line	1	4.2		5.7	nde.		
		Vcc _{GT} Loadline	U- 2 Core GT2, GT1	20-	—		3.1			7, 9
	Processor) slope		U- 4 Core GT2 (U- 4 Core)	—	—		3.1			10
U.			U- 2 Core GT3+OPC	-	—)	1		
	AC_LL (Y/U- Processors)	AC Loadline	U-Processor Line	_	_	Sam	ne as Max DC_LL (up to 1MHz)	mΩ	7,9 10,1
AC_LL (Y- Processors) T_OVS_MAX V_OVS_MAX		AC Loadline	Y/AML-Y22 -Processor Line	_	-	• 3MHz – (freque	3MHz: 5.7 10MHz: Increasir ncy) from 5.7 to 1 - 40MHz: 12.1	ng linearly with log 2.1	mΩ	7,9 10,1
		Max Overshoot time	-	eg v	n <u>o</u> e.		10	4 undern	μs	
		Max Overshoot	- defi	-	_		70	fineo	mV	

id undefined undefined Processor Graphics (Vcc_{GT} and Vcc_{GTX}) Supply DC Voltage and Current Specifications (Sheet 2 of 2) Table 7-3.

Notes:

Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.

2. Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. This differs from the VID employed by the processor during a power or thermal management event (Intel Adaptive Thermal Monitor, Enhanced Intel SpeedStep Technology, or low-power states).

- The voltage specification requirements are measured across Vcc_{GT_SENSE} and Vss_{GT_SENSE} as near as possible to the processor with an oscilloscope set to 100-MHz bandwidth, 1.5 pF maximum probe capacitance, and 1 M Ω minimum impedance. The maximum length of 3. ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe. PSx refers to the voltage regulator power state as set by the SVID protocol. 4.
- Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and cannot be 5. altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. This differs from the VID employed by the processor during a power or thermal management event (Intel Adaptive Thermal Monitor, Enhanced Intel SpeedStep Technology, or low-power states).
- 6. N/A

LL measured at sense points.

Operating voltage range in steady state. 8.

LL specification values should not be exceeded. If exceeded, power, performance and reliability penalty are expected. Load Line (AC/DC) should be measured by the VRTT tool and programmed accordingly using the BIOS Load Line override setup options. AC/DC Load Line BIOS programming directly affects operating voltages (AC) and power measurements (DC). A superior board design 9. 10. with a shallower AC Load Line can improve on power, performance, and thermals compared to boards designed for POR impedance. 11. N/A

For merged GT/GTx rails the sense point need to be taken from Vcc_{GT}_SENSE/VSSGT_SENSE, the Vcc_{GTx SENSE}/Vss_{GTx SENSE} should be 12. unconnected (not connected).

For more details on AML-Y22 loadline target, refer to Power Integrity Model Set Doc ID# 597383... 13. e - - - A emotestimed undefined undefined undefined undefined undefined undefined undefined ed undefined undefine



ned undefined undefined **V**_{DDQ} DC Specifications 7.2.1.3

Table 7-4. Memory Controller (V_{DDO}) Supply DC Voltage and Current Specifications

Parameter	Segment	Min	⊘Тур	Max	Unit	Note ¹	
Processor I/O supply voltage for DDR3L/-RS	All	Тур-5%	1.35	Typ+5%	v	3,4,5	4efine
Processor I/O supply voltage for LPDDR3	All	Typ-5%	1.20	Typ+5%	v	3, 4, 5	10-
Processor I/O supply voltage for DDR4	All	Typ-5%	1.20	Typ+5%	V	3, 4, 5	
VDDQ Tolerance	All		AC+DC:± 5	5	%	3, 4, 6	
Max Current for V _{DDQ} Rail	U	—	_	2	Δ	2	
	_	-		er		2	
Max Current for V _{DDQ} Rail	Y/AML-Y22	-	. –JN	2			
(LPDDK3)	U	-	eo_	2	А	2	define
nde	_	(i	_				2015
Max Current for V _{DDQ} Rail (DDR4)	U	JUnoc	_	2.8	А	2	deth
	Processor I/O supply voltage for DDR3L/-RS Processor I/O supply voltage for LPDDR3 Processor I/O supply voltage for DDR4 VDDQ Tolerance Max Current for V _{DDQ} Rail (DDR3L/-RS) Max Current for V _{DDQ} Rail (LPDDR3) Max Current for V _{DDQ} Rail	Processor I/O supply voltage for DDR3L/-RS All Processor I/O supply voltage for LPDDR3 All Processor I/O supply voltage for DDR4 All VDDQ Tolerance All Max Current for V _{DDQ} Rail (LPDDR3) U Max Current for V _{DDQ} Rail (LPDDR3) U Max Current for V _{DDQ} Rail U Max Current for V _{DDQ} Rail U	Processor I/O supply voltage for DDR3L/-RS All Typ-5% Processor I/O supply voltage for LPDDR3 All Typ-5% Processor I/O supply voltage for DDR4 All Typ-5% VDDQ Tolerance All Typ-5% VDDQ Tolerance All Max Current for V _{DDQ} Rail (LPDDR3) U Max Current for V _{DDQ} Rail U Max Current for V _{DDQ} Rail U Max Current for V _{DDQ} Rail U U Max Current for V _{DDQ} Rail U	Processor I/O supply voltage for DDR3L/-RSAllTyp-5%1.35Processor I/O supply voltage for LPDDR3AllTyp-5%1.20Processor I/O supply voltage for DDR4AllTyp-5%1.20VDDQ ToleranceAllTyp-5%1.20Max Current for V _{DDQ} Rail (LPDDR3)UMax Current for V _{DDQ} Rail (LPDDR3)Y/AML-Y22Max Current for V _{DDQ} Rail (LPDDR3)UMax Current for V _{DDQ} Rail (LPDDR3)UMax Current for V _{DDQ} Rail (LPDDR3)UUMax Current for V _{DDQ} Rail (LPDDR3)U	Processor I/O supply voltage for DDR3L/-RSAllTyp-5%1.35Typ+5%Processor I/O supply voltage for LPDDR3AllTyp-5%1.20Typ+5%Processor I/O supply voltage for DDR4AllTyp-5%1.20Typ+5%VDDQ ToleranceAllTyp-5%1.20Typ+5%Max Current for V _{DDQ} Rail (LPDDR3)U2Max Current for V _{DDQ} Rail (LPDDR3)Y/AML-Y222Max Current for V _{DDQ} Rail (LPDDR3)U2Max Current for V _{DDQ} Rail (LPDDR3)U2	Processor I/O supply voltage for DDR3L/-RSAllTyp-5%1.35Typ+5%VProcessor I/O supply voltage for LPDDR3AllTyp-5%1.20Typ+5%VProcessor I/O supply voltage for DDR4AllTyp-5%1.20Typ+5%VVDDQ ToleranceAllTyp-5%1.20Typ+5%VMax Current for V_DDQ Rail (LPDDR3)U2AMax Current for V_DDQ Rail (LPDDR3)Y/AML-Y222AMax Current for V_DDQ Rail (LPDDR3)U2AMax Current for V_DDQ Rail (LPDDR3)U2A	Processor I/O supply voltage for DDR3L/-RS All Typ-5% 1.35 Typ+5% V 3,4,5 Processor I/O supply voltage for LPDDR3 All Typ-5% 1.20 Typ+5% V 3,4,5 Processor I/O supply voltage for DDR4 All Typ-5% 1.20 Typ+5% V 3,4,5 VDDQ Tolerance All Typ-5% 1.20 Typ+5% V 3,4,6 Max Current for V _{DDQ} Rail (LPDDR3) U - - 2 A 2 Max Current for V _{DDQ} Rail Y/AML-Y22 - - 2 A 2 Max Current for V _{DDQ} Rail U - - 2 A 2 Max Current for V _{DDQ} Rail U - - 2 A 2 Max Current for V _{DDQ} Rail U - - 2 A 2 Max Current for V _{DDQ} Rail U - - 2 A 2

Notes:

Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These 1. specifications will be updated with characterized data from silicon measurements at a later date.

2. The current supplied to the DIMM modules is not included in this specification.

Includes AC and DC error, where the AC noise is bandwidth limited to under 100 MHz, measured on package pins. No requirement on the breakdown of AC versus DC noise. 3.

4. 5. The voltage specification requirements are measured as near as possible to the processor with an oscilloscope set to 100-MHz bandwidth, 1.5 pF maximum probe capacitance, and 1 M Ω minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe. For Voltage less than 1v, TOB will be 50 mv. 6.

7.2.1.4 Vcc_{SA} DC Specifications

System Agent (Vcc_{SA}) Supply DC Voltage and Current Specifications (Sheet 1 of 2) **Table 7-5.**

7.2.1	.4 Vc	c _{SA} DC Specifications			adefinee			ined v
Table	7-5. Sy of	stem Agent (Vcc _{SA}) Supply 2)	y DC \	/oltag	e and Current Specifications (She	et 1	unde	
mbol	Parameter	Segment	Min	Тур	Max	Unit	Note ^{1,2}	
4 e	Voltage for	Y/AML-Y22 -Processor Line	0	-	1.52			
essors)	Agent	U-Processor Line	0	-	1.52	v	3, 5	
Un	VCCGA	U/Y/AML-Y22 -Processor Lines	0	-	±20	mV	3	
CCSA	Tolerance	- du	0	-	. uno	%	3, 11	
		Y/AML-Y22 -Processor Line	-	-	4.1			2
	Max Current	U- 2 Core GT2	-	-	4.5	^	9	ineu
X_VCCSA	Rail	U- 2 Core GT3+OPC	-	-	5.1		10	
		U- 4 Core GT2 (U- 4 Core)	-	-	6	1	JUN	
I	Vcc _{SA}	Y/AML-Y22-Processor Line	-	14	18	mQ	678	
	Loadline	U/U- 4 Core Processor Line		100	10.3	11132	0,7,0	
L	AC Loadline	U/-Processor Line	ned	-	Same as Max DC_LL (up to 1MHz)	mΩ	6, 7, 8,12	
1 une	AC Loadline	Y/AML-Y22 -Processor Line	-	-	 1MHz - 2MHz: Increasing linearly with log (frequency) from 18 to 42.6 2MHz - 40MHz: 42.6 	mΩ	6, 7, 8,12	
		d undefilt			undefines		6	efined
	, un	define		6	stined	nije.	ed une	
110	efined .	unde	fined	Une	Datasheet, Volum	e 1 of 2		
	mbol (ssors) (ccsa (x_vccsa) L	Table 7-5. Sy of mbol Parameter Voltage for the System Agent CCSA VCcSA Tolerance X_VCCSA Max Current for V _{CCSA} Rail L VCcSA Loadline L AC Loadline L AC Loadline	Table 7-5. System Agent (Vcc _{SA}) Supply of 2)mbolParameterSegmentModeVoltage for the System AgentY/AML-Y22 -Processor LineU-Processor LineU-Processor LineUCCSAU/Y/AML-Y22 -Processor LineCCSAVcc _{SA} ToleranceU/Y/AML-Y22 -Processor LineX_VCCSAV/CCSA ToleranceU/Y/AML-Y22 -Processor LineX_VCCSAMax Current for V _{CCSA} RailY/AML-Y22 -Processor LineU- 2 Core GT2 U- 2 Core GT3+OPCU- 2 Core GT3+OPCLVcc _{SA} LoadlineY/AML-Y22-Processor LineLAC LoadlineU/- Processor LineLAC LoadlineU/-Processor LineLAC LoadlineY/AML-Y22 -Processor Line	Table 7-5.System Agent (Vcc _{SA}) Supply DC V of 2)mbolParameterSegmentMinVoltage for the System AgentY/AML-Y22 -Processor Line0U-Processor Line0U/Y/AML-Y22 -Processor Line0CCSAVcc _{SA} ToleranceU/Y/AML-Y22 -Processor Line0X_VCCSAV/CcSA ToleranceU/Y/AML-Y22 -Processor Line0X_VCCSAMax Current for VccSA RailY/AML-Y22 -Processor Line-U- 2 Core GT2U- 2 Core GT2U- 2 Core GT2 (U- 4 Core)-LVccSA LoadlineY/AML-Y22-Processor Line-LAC LoadlineU/-Processor Line-LAC LoadlineU/-Processor Line-AC LoadlineV/AML-Y22 -Processor Line-	Table 7-5.System Agent (Vcc _{SA}) Supply DC Voltag of 2)mbolParameterSegmentMinTypAgentV/AML-Y22 -Processor Line0-Voltage for the System AgentV/AML-Y22 -Processor Line0-CCSAVcc _{SA} ToleranceU/Y/AML-Y22 -Processor Line0- χ_{x_vccSA} Max Current for VccsA RailY/AML-Y22 -Processor Line0-U- 2 Core GT2U- 2 Core GT2U- 4 Core GT2 (U- 4 Core)LVccsA LoadlineY/AML-Y22-Processor Line-14U/U- 4 Core Processor LineLAC LoadlineU/-Processor LineLAC LoadlineU/-Processor LineLAC LoadlineV/AML-Y22 -Processor LineLAC LoadlineV/AML-Y22 -Processor Line	Table 7-5. System Agent (Vcc _{SA}) Supply DC Voltage and Current Specifications (She of 2)mbolParameterSegmentMinTypMaxMoltage for the System AgentY/AML-Y22 -Processor Line0-1.52U-Processor Line0-1.52CCSA Vcc_{SA} ToleranceU/Y/AML-Y22 -Processor Lines0-4.10V V_{2SA} ToleranceU/Y/AML-Y22 -Processor Line $X_{2}VCCSA$ Wcc_{SA} ToleranceU/Y/AML-Y22 -Processor Line V_{2SA} Rail Vcc_{SA} U-2 Core GT24.1U-2 Core GT24.5-U-2 Core GT26-U-4 Core GT2 (U-4 Core)6-L Vcc_{SA} LoadlineU/U-4 core Processor Line-1418U/U-4 Core Processor LineSame as Max DC_LL (up to 1MHz)L AC Loadline $V/AML-Y22$ -Processor LineSame as Max DC_LL (up to 1MHz)L AC Loadline $V/AML-Y22$ -Processor LineL AC Loadline $V/AML-Y22$ -Processor LineL AC Loadline $V/AML-Y22$ -Processor LineL AC Loadline $V/AML-Y22$ -Processor LineL AC Loadline $V/$	Table 7-5. System Agent (Vcc _{SA}) Supply DC Voltage and Current Specifications (Sheet 1mbolParameterSegmentMinTypMaxUnitAgentV/AML-Y22 -Processor Line0-1.52VSsors)VU-Processor Line0-1.52VCCSAVcc _{SA} ToleranceU/Y/AML-Y22 -Processor Line0-4.10mV χ_{VCCSA} V/Cc _{SA} ToleranceV/AML-Y22 -Processor Line0-4.1MV χ_{VCCSA} V/Cc _{SA} ToleranceV/AML-Y22 -Processor Line4.1MV χ_{VCCSA} V/Cc _{SA} ToleranceV/AML-Y22 -Processor Line4.5A χ_{VCCSA} V/Cc _{SA} LoadlineV/AML-Y22 -Processor Line6MNLVcc _{SA} LoadlineV/AML-Y22-Processor Line10.3mQLAC LoadlineU/-Processor LineSame as Max DC_LLL (up to 1MHz)mQLAC LoadlineV/AML-Y22 -Processor Line10.3mQ	Table 7-5. System Agent (Vcc _{SA}) Supply DC Voltage and Current Specifications (Sheet 1 of 2)mbolParameterSegmentMinTypMaxUnitNote ^{1,2} Notage for the System AgentV/AML-Y22 -Processor Line0-1.52V3, 5VCCSA toleranceU/Y/AML-Y22 -Processor Line0-1.52V3, 5VCCSA RailU/Y/AML-Y22 -Processor Line0-4.13X_VCCSA RailV/AML-Y22 -Processor Line4.19U-2 Core GT24.549U-2 Core GT2 (U- 4 Core)6U-2 Core GT2 (U- 4 Core)6U-2 Core GT2 (U- 4 Core)10.3m06, 7, 8LVCcSA LoadlineU/U-4 Core Processor LineSame as Max DC_LL (up to 1MHz)m06, 7, 8,12LAC LoadlineU/-Processor Line6, 7, 8,12LAC LoadlineV/AML-Y22 -Processor Line6, 7, 8,12LAC LoadlineV/AML-Y22 -Processor Line6, 7, 8,12LAC LoadlineV/AML-Y22 -Processor Line6, 7, 8,12LAC LoadlineV/AML-Y22 -Processor Line6, 7, 8,12LAC LoadlineV/AML-Y22 -Pro



led undefined undefined stined System Agent (Vcc_{SA}) Supply DC Voltage and Current Specifications (Sheet 2 Table 7-5. of 2)

Symbol	Parameter	er Segment Min		Тур	Max				Note ^{1,}
		U/Y-Processor Lines			I _L <=0.5	0.5 <il<icc<sub>TDC</il<icc<sub>	I _{CCTDC} <i<sub>L<icc<sub>MAX</icc<sub></i<sub>		
		PSO	-	-	+30/-10	±10	±15		nip.
Ripple	Ripple Tolerance	PS1	—	- ~	+30/-10	±15	±15	mV	3, 4
	16/11	PS2	-		+30/-10	+30/-10	+30/-10	90.	
	unos	PS3	-36	<u> </u>	+30/-10	+30/-10	+30/-10		
T_OVS_MAX	Max Overshoot time	-	UI.	_		10	od under	μs	
V_OVS_MAX	Max Overshoot	- Inden	-	_		70	nee	mV	

Notes:

Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be 1. updated with characterized data from silicon measurements at a later date.

2. Long term reliability cannot be assured in conditions above or below Max/Min functional limits.

The voltage specification requirements are measured across Vcc_{SA-SENSE} and Vss_{SA-SENSE} as near as possible to the processor with an oscilloscope set to 100-MHz bandwidth, 1.5 pF maximum probe capacitance, and 1 M Ω minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe. 3. 4 PSx refers to the voltage regulator power state as set by the SVID protocol.

Vcc_{SA} voltage during boot (Vboot)1.05V for a duration of 2 seconds. 5.

LL measured at sense points.

6. 7. LL specification values should not be exceeded. If exceeded, power, performance and reliability penalty are expected.

8. Load Line (AC/DC) should be measured by the VRTT tool and programmed accordingly using the BIOS Load Line override setup options. AC/DC Load Line BIOS programming directly affects operating voltages (AC) and power measurements (DC). A superior board design with a shallower AC Load Line can improve on power, performance, and thermals compared to boards designed for POR impedance.

9

undermed underme IPU designs with U-Processor Line Pentium/Celeron require additional 0.5A, SA Icc_{MAX}=5A. U-Processor Line GT2+OPC 28W IPU designs will require additional 2A, SA Icc_{MAX} when using IPU=7.1AFor Voltage less than 1V, TOB will be 50 10. <u>. 10# 5</u> mV.

For more details on AML-Y22 loadline target, refer to Power Integrity Model Set Doc ID# 597383. 11.

Datasheet, Volume 1 of 2 ...

Electrical Specifications ned undefin



ted undefined undefined Vcc_{IO} DC Specifications 7.2.1.5

Processor I/O (Vcc_{IO}) Supply DC Voltage and Current Specifications Table 7-6.

Jer.	Symbol	Parameter	Segment	Min	Тур	Max	Unit	Note ^{1,2}	- 61	
		Voltage for the memory controller	Y/AML-Y22	Indel	0.85/0.95	_		3, 4, 5,	definec	
	Vcc _{IO}	and shared cache	U O	_	0.95		V	6	TUC	
		96,	- AUL	-	—	—		ine ^o		
	TOB _{VCCIO}	Vcc _{IO} Tolerance	All +/-5 (AC + D Up to 1			ipple)	%	3, 8		
	Icc	Max Current for V _{CCIO} Rail	Y/AML-Y22		_	3	А			
, un	Icc _{MAX_VCCIO}	Max Current for V _{CCIO} Kan	U	_	-	3.1	^			
neo	T_OVS_MAX	Max Overshoot time	All	_	- "nõ	100	μS	7		
efiii	V_OVS_MAX	Max Overshoot at TDP	All	—	à à.	20	mV	7		
70	 Notes: Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date. Long term reliability cannot be assured in conditions above or below Max/Min functional limits. The voltage specification requirements are measured across Vcc_{IO_SENSE} and Vss_{IO_SENSE} as near as possible to the processor with an oscilloscope set to 100-MHz bandwidth, 1.5 pF maximum probe capacitance, and 1 MΩ minimum 									

Notes:

The voltage specification requirements are measured across Vcc_{IO-SENSE} and Vss_{IO-SENSE} as near as possible to the processor with an oscilloscope set to 100-MHz bandwidth, 1.5 pF maximum probe capacitance, and 1 M Ω minimum 3. impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.

- For low BW bus connection between processor and PCH -> Vcc_{IO} =0.85V. 4. 5.
- For high BW bus connection between processor and PCH -> Vc_{IO} =0.85V. For high BW bus connection between processor and PCH -> Vc_{IO} =0.95V. For KBL-Y and AML Y-Processor Line, Setting Vc_{IO} to 0.95V may lead to a power penalty up to 250mW. OS occurs during power on only, **not** during normal operation. For Voltage less than 1v, TOB will be +/-50mV (AC + DC + Ripple) up to 1 MHz 6.
- 7.
- 8.

7.2.1.6 VCCOPC DC Specifications

undefined undefined un OPC VR output voltage is fixed to 1V, the processor can drive VR to LPM (Low Power Mode) which sets VR output to 0V using ZVM# signal as shown in the following table.

Table 7-7. VCC_{OPC} Voltage levels

ZVM# State	VCC _{OPC}	Units				
0	0	V				
1	1.0	v				

Processor OPC (Vcc_{OPC}) Supply DC Voltage and Current Specifications (Sheet **Table 7-8.** 1 of 2)

Symbol	Parameter	Segment	Min	Тур	Max	Unit	Note ^{1,2}
Vcc _{OPC}	Voltage for the on-package cache	Processor Line w/OPC	, defi	1.0	-	V	311120
TOB _{VCCOPC}	Vcc _{OPC} Tolerance	Processor Line w/OPC	<u>}</u>	AC+	DC:± 5	%	3, 5
ICCMAX_VCCOPC	Max Current for V _{CCOPC} Rail	Processor Line w/OPC	_	-	3.2	A	
T_OVS_MAX	Max Overshoot time	All	—	-	100	μS	4
V_OVS_MAX	Max Overshoot at TDP	All	_	-	20	mV	4
112	undefined under	undefined	undef	ined un	Datash	eet, Vo	lume 1 of 2



ad undefined undefin Processor OPC (Vcc_{OPC}) Supply DC Voltage and Current Specifications (Sheet Table 7-8. 2 of 2)

	2 OF 2)				ger.			
Symbol	Parameter	Segment	Min	Тур	Max	Unit	Note ^{1,2}	211
specific 2. Long te 3. The vo process impeda system 4. OS occ	otherwise noted, all specifications ations will be updated with charact rm reliability cannot be assured in tage specification requirements an or with an oscilloscope set to 100- nce. The maximum length of groun is not coupled into the oscilloscop- urs during power on only, not durin cage less than 1V, TOB will be 50 m	erized data from si conditions above o e measured across MHz bandwidth, 1. nd wire on the prob e probe. ng normal operation	ilicon mea or below M Vcc _{OPC-SI} 5 pF maxi oe should	asurement lax/Min fu _{ENSE} and \ imum pro	s at a later date. nctional limits. /ss _{OPC-SENSE} as near be capacitance, and 3	as possible 1 MΩ minimu	to the	defined L.
÷.		113				e _o		-

7.2.1.7 **VCCEOPIO DC Specifications**

undefined undefined ut Vcc_{EOPIO} may be connected to OPC VR. The processor can drive VR to LPM (Low Power Mode) which sets VR output to 0V using ZVM# signal (as shown in Table 7-9, "VCCFOPIO Voltage levels (separate VR)").

Table 7-9. VCC_{EOPIO} Voltage levels (separate VR)

	ZVM# sta	ate	MSM# state		VCCE	OPIO		Un	its	
	sine o		Х	ed	()		١	/	S
	1		1	ill'	1	.0		١	/	0
ed un				nas					den	-
16tine	Table 7-10.	Process	sor EOPIO (Vo	C _{EOPIO}) S	Supply	DC V	oltage a	and Curr	ent Spec	ifi
unas	Symbol		Parameter	Segm	ent	Min	Тур	IL I	Мах	l
	Vcc .	Voltage	for the EOPIO				-0-			+

Table 7-10. Processor EOPIO (Vcc_{EOPIO}) Supply DC Voltage and Current Specifications

Table 7-10 .	Processor EOPIO (Vcc	EOPIO) Supp	Iy DC V	oltage a	ind Current Spec	ificati	ons	
Symbol	Parameter	Segment	Min	Тур	Max	Unit	Note ^{1,2}	ed '
Vcc _{EOPIO}	Voltage for the EOPIO interface		_	1.0	_	V	3	ndefill
TOB _{VCCEOPIO}	Vcc _{EOPIO} Tolerance	U-Processor	sin ^e	AC+	-DC:± 5	%	3, 5	0.
Icc _{MAX_VCCEOPIO}	Max Current for V _{CCEOPIO} Rail	Line GT3 with OPC	967.	_	2	А	SIL	
T_OVS_MAX	Max Overshoot time		-	—	100	μS	4	
V_OVS_MAX	Max Overshoot at TDP	cineo	-	—	20	mV	4	
								1

Notes:

Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.

2. Long term reliability cannot be assured in conditions above or below Max/Min functional limits.

The voltage specification requirements are measured across $Vcc_{EOPIO-SENSE}$ and $Vss_{EOPIO-SENSE}$ as near as possible to the processor with an oscilloscope set to 100-MHz bandwidth, 1.5 pF maximum probe capacitance, and 1 M Ω minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.

OS occurs during power on only, **not** during normal operation. For Voltage less than 1V, TOB will be 50 mV. 4.

5.

Vcc_{OPC 1p8} DC Specifications 7.2.1.8

Table 7-11. Processor OPC (Vcc_{OPC_1p8}) Supply DC Voltage and Current Specifications

Symbol	Parameter	Segment	Min	Тур	Max	Unit	Note ^{1,2}	
Vcc _{OPC_1p8}	Voltage for the on-package cache	U-Processor	_	1.8	ed un	V	3	2
TOB _{VCC_OPC_1p8}	Vcc _{OPC_1p8} Tolerance	Line GT3 with OPC		AC+D	C:± 5	%	3, 4	cineu
ICC _{MAX_VCC_OPC_1p8}	Max Current for V _{CC_OPC_1p8} Rail		_	.140	50	mA		den
Datasheet, Volume 1	of 2	affined und	stine		d undefi	ned	undefin	13



ed undefined undefine Table 7-11. Processor OPC (Vcc_{OPC_1p8}) Supply DC Voltage and Current Specifications

Symbol	Parameter	Segment	Min	Тур	Мах	Unit	Note ^{1,2}	
Notes:	ise noted, all specifications in this	table are based o	n estimat	es and sim	ulations or emp	pirical data	These	d une
specifications	will be updated with characterized ability cannot be assured in condit	l data from silicon	measure	ments at a	later date.			sineo
3. The voltage sp	pecification requirements are meas	sured as near as p	ossible to	the proces	ssor with an osc			dell
	h, 1.5 pF maximum probe capacit obe should be less than 5 mm. En							UIL
 probe. For Voltage less 	ss than 1V. TOB will be 50 mV.	7641					siner	

7.2.1.9 Vcc_{ST} DC Specifications

Table 7-12. Vcc Sustain (Vcc_{ST}) Supply DC Voltage and Current Specifications

Symbol	Parameter	Segment	Min	Тур	Max	Units	Notes 1,2	
/cc _{ST}	Processor Vcc Sustain supply voltage	All	_	1.0	_	V	3	ined '
ГОВ _{ST}	Vcc _{ST} Tolerance	All	2.	AC+DC:± 5		%	3, 4	dell.
	sine	Y/AML-Y22-Processor Line	e e e	—				unc
cc _{MAX_ST}	Max Current for Vcc _{st}	U-Processor Line	<u> </u>	—	60	mA	e o	
ed u		U-Processor Line (U- 4 Core)	_	_			defin	

Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date. 2. Long term reliability cannot be assured in conditions above or below Max/Min functional limits.

3. The voltage specification requirements are measured on package pins as near as possible to the processor with an oscilloscope set to 100-MHz bandwidth, 1.5 pF maximum probe capacitance, and 1 MΩ minimum impedance. The maximum simed undefined length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.For Voltage less than 1V, TOB will be 50 mV.

Table 7-13. Vcc Sustain Gated (Vcc_{STG}) Supply DC Voltage and Current Specifications

		05					
Symbol	Parameter	Segment	Min	Тур	Max	Units	Notes 1,2
Vcc _{STG}	Processor Vcc Sustain supply voltage	All defined	_	1.0	-	N	3
TOB _{STG}	Vcc _{STG} Tolerance	All		AC+DC:± 5	~9e	%	3, 4
		Y/AML-Y22 -Processor Line		-	2 UN		
Icc _{MAX_STG}	Max Current for Vcc _{STG}	U-Processor Line	_		20	mA	
MAX_STO	d unosid	U-Processor Line (U- 4 Core)	_	nden			

Notes:

Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date. Long term reliability cannot be assured in conditions above or below Max/Min functional limits. 1.

2. The voltage specification requirements are measured on package pins as near as possible to the processor with an 3. oscilloscope set to 100-MHz bandwidth, 1.5 pF maximum probe capacitance, and 1 M Ω minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.

e a undefined undefined undefined

For Voltage less than 1V, TOB will be 50 mV. 4. undefined undefined undefined undefined

Datasheet, Volume 1 of 2 -4 undefined



7.2.1.10 Vcc_{PLL} DC Specifications

Table 7-14. Processor PLL (Vcc_{PLL}) Supply DC Voltage and Current Specifications

Symbol	Parameter	Segment	Min	Тур	Мах	Unit	Notes ^{1,2}
Vcc _{PLL}	PLL supply voltage (DC + AC specification)	All	. Inde	1.0	_	V	3,7
TOB _{VCCPLL}	Vcc _{PLL} Tolerance	All	VCC _{PLLma}	ax > AC+D	C > VCC _{PLLmin}	V	3,4,5,6,7
LPF UNO	Noise Filtering for Vcc _{PLL}	All	the low p cut-o	ass filter r ff frequend	behavior like is equirements are cy and -20dB/De higher frequence	e 150KHz ecade	5,6
C.		Y/AML-Y22 -Processor Line	_	_	100		
Icc _{MAX_VCCPLL}	Max Current for Vcc _{PLL} Rail	U-Processor Line	-	_	130	mA	
	stinec	U-Processor Line (U- 4 Core)	—	-eq	130		

1. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.

2. Long term reliability cannot be assured in conditions above or below Max/Min functional limits. 3.

The voltage specification requirements are measured on package pins as near as possible to the processor with an oscilloscope set to 100-MHz bandwidth, 1.5 pF maximum probe capacitance, and 1 M Ω minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.For Voltage less than 1v, TOB will be 50 mv.Vcc_{PLL} max noise freq 0.5 MHz. LPF should implement after making sure VCCPLL AC+DC are inside TOB_{VCCPLL} limits

- 5. Should be measured and verified prior to LPF assembly

Table 7-15. Processor PLL_OC (Vcc_{PLL_OC}) Supply DC Voltage and Current Specifications

Symbol	Parameter	Segment	Min	Тур	Max	Un it	Notes ^{1,2}
Vcc _{PLL_OC}	PLL_OC supply voltage (DC + AC specification)	All	-	V _{DDQ}	_	v	efil380
TOB _{CCPLL_OC}	Vcc _{PLL_OC} Tolerance	All	A	C+DC:±	5	%	3,4
9er		Y/AML-Y22 -Processor Line	-	-	100		
Tas	Max Current for	U-Processor Line - 2 Core GT2	-	726	100		
ICC _{MAX_VCCPLL_OC}	Vcc _{PLL_OC} Rail	U-Processor Line - 4 Core GT2 (U- 4 Core)	-	JAU	100	mA	
	213-	U-Processor Line - 2 Core GT3+OPC	-eÔ	_	120		

Notes:

Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These 1. specifications will be updated with characterized data from silicon measurements at a later date. Long term reliability cannot be assured in conditions above or below Max/Min functional limits.

2.

The voltage specification requirements are measured on package pins as near as possible to the processor with an 3. oscilloscope set to 100-MHz bandwidth, 1.5 pF maximum probe capacitance, and 1 M Ω minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.

For Voltage less than 1V, TOB will be 50 mV. e -----





led undefined undefined

	intel	ine undefined			Electri	ical Spe	cifications	5
. inf	7.2.2	Processor Interfaces DC Specif	ficatio	าร				
		DDR3L/-RS DC Specifications	ing.	ned un	961			
	Symbol	DDR3L/-RS Signal Group DC Specification Parameter	Y and	U-Process		Units	Notes ¹	undefit
	VIL	Input Low Voltage	Min —	Тур	Max 0.43* V _{DDO}	vÒ	2, 4, 8,	
27.	V _{IH}	Input High Voltage	0.57* V _{DDQ}	_		v	3, 4, 8, 9	
du	R _{ON_UP/DN(DQ)}	DDR3L/-RS Data Buffer pull-up/down Resistance		Trainable	'ger.	Ω	10	
	R _{ODT(DQ)}	DDR3L/-RS On-die termination equivalent resistance for data signals		Trainable		Ω	10	
	V _{ODT(DC)}	DDR3L/-RS On-die termination DC working point (driver set to receive mode)	0.45* V _{DDQ}	0.5* V _{DDQ}	0.55* V _{DDQ}	V	10	4efine
	R _{ON_UP/DN(CK)}	DDR3L/-RS Clock Buffer pull-up/down Resistance	0.8*Typ	26	1.2*Typ	Ω	5, 10	ino
	R _{ON_UP/DN(CMD)}	DDR3L/-RS Command Buffer pull-up/down Resistance	0.8*Typ	20	1.2*Typ	Ω	10	
	R _{ON_UP/DN(CTL)}	DDR3L/-RS Control Buffer pull-up/down Resistance	0.8*Typ	20	1.2*Typ	Ω	5, 10	
	R _{ON_UP/DN} (DDR_VTT_CNTL)	System Memory Power Gate Control Buffer Pull-Up/ down Resistance	40	-	140	Ω	0.0	
tined u	I _{LI}	Input Leakage Current (DQ, CK) 0 V 0.2*V _{DDQ} 0.8*V _{DDQ}	_		indefin	mA		
	DDR0_Vref_DQ DDR1_Vref_DQ DDR_Vref_CA	VREF output voltage	Trainable	V _{DDQ} /2	Trainable	v	9,11	adefin
	DDR_RCOMP[0]	ODT resistance compensation	eo.			Ω	6	UI.
	DDR_RCOMP[1]	Data resistance compensation		values are logy deper		Ω	6	0
	DDR_RCOMP[2]	Command resistance compensation	topo	iogy deper	ident.	Ω	6	

Notes:

Unless otherwise noted, all specifications in this table apply to all processor frequencies.

V_{IL} is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value. 2.

VIH is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value. 3.

4. $v_{IH}^{''}$ and V_{IL} may experience excursions above V_{DDO} . However, input signal drivers should comply with the signal quality specifications.

5. This is the pull up/down driver resistance after compensation. Note that BIOS power training may change these values significantly based on margin/power trade-off.

6. For U/Y Processors DDR_RCOMP resistance should be provided on the system board with ±1% resistors. DDR_RCOMP resistors are connected to V_{SS} . DDR_VREF is defined as $V_{DDQ}/2$ for DDR3L/-RS R_{ON} tolerance is preliminary and might be subject to change. Processor may be damaged if V_{IH} exceeds the maximum voltage for extended periods. Final value determined by BIOS power training, values might vary between bytes and/or units.

7.

8.

9.

10.

- 11.
- The value will be set during the MRC boot training within the specified range. DDR0_Vref_DQ Not in use in DDR4, DDR1_Vref_DQ = DDR4_CA_ch1, DDR_Vref_CA = DD4_CA_ch0. e a survey of the survey of th 12.

ined undefined ! Datasheet, Volume 1 of 2 -4 undefined

defin

d undefined u

ndefined unde 7.2.2.2 LPDDR3 DC Specifications

Table 7-17. LPDDR3 Signal Group DC Specifications

Symbol	DDR3 Signal Group DC Specification	S U/U- 4 Core and AML Y- Processor Line				Note	tefined
sine		Min	Тур	Max	Unit	1012	de.
VIL	Input Low Voltage	_	_	0.43*V _{DDQ}	V	2, 4, 8, 9	
VIH	Input High Voltage	0.57*V _{DDQ}	_	_	V	3, 4, 8, 9	
R _{ON_UP/DN(DQ)}	LPDDR3 Data Buffer pull-up/ down Resistance		Trainable		Ω	11	
R _{ODT(DQ)}	LPDDR3 On-die termination equivalent resistance for data signals		Trainable	stined	Ω	11	
V _{ODT(DC)}	LPDDR3 On-die termination DC working point (driver set to receive mode)	$0.45*V_{DDQ}$	0.5*V _{DD} Q	0.55*V _{DDQ}	V	9	
R _{ON_UP/DN(CK)}	LPDDR3 Clock Buffer pull-up/ down Resistance	0.8*Typ	40	1.2*Typ	Ω	5, 11	
R _{ON_UP/DN(CMD)}	LPDDR3 Command Buffer pull-up/ down Resistance	0.8*Typ	40	1.2*Typ	Ω	11	define
R _{ON_UP/DN(CTL)}	LPDDR3 Control Buffer pull-up/ down Resistance	0.8*Typ	23	1.2*typ	Ω	5, 11	no
R _{ON_UP/DN} (DDR_VTT_CNTL)	System Memory Power Gate Control Buffer Pull- Up Resistance	40	_	140	Ω	rine	
I _{LI}	Input Leakage Current (DQ, CK) OV 0.2* V _{DDQ} 0.8*V _{DDQ}	_	-	0.75	mA	-	
I _{LI}	Input Leakage Current (CMD,CTL) 0V 0.2*V _{DDQ} 0.8*V _{DDQ}	nde	tined u	0.9	mA	-	defin
DDR0_VREF_DQ DDR1_VREF_DQ DDR_VREF_CA	VREF output voltage	Trainable	V _{DDQ} /2	Trainable	v	12,13	JUG
DDR_RCOMP[0]	ODT resistance compensation	DOOMD .			Ω	6	
DDR_RCOMP[1]	Data resistance compensation	RCOMP value	es are mem dependent.		Ω	6	
DDR_RCOMP[2]	Command resistance compensation				Ω	6	

Notes:

undefined und

undefined unt

Unless otherwise noted, all specifications in this table apply to all processor frequencies. 1

2. V_{IL} is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.

 V_{1H}^{T} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value. 3. 4.

V_{IH} and V_{IL} may experience excursions above V_{DDO}. However, input signal drivers should comply with the signal quality specifications.

5. This is the pull up/down driver resistance after compensation. Note that BIOS power training may change these values significantly based on margin/power trade-off.

6. 7. DDR_RCOMP resistance should be provided on the system board with ±1% resistors. DDR_RCOMP resistors are to V_{SS}. lefinec DDR_VREF is defined as $V_{DDQ}/2$ for LPDDR3 R_{ON} tolerance is preliminary and might be subject to change. The value will be set during the MRC boot training within the specified range.

8.

- 9.
- 10. Processor may be damaged if V_{IH} exceeds the maximum voltage for extended periods.

Final value determined by BIOS power training, values might vary between bytes and/or units. 11.

- 12.
- VREF values determined by BIOS training, values might vary between units. DDR0_Vref_DQ Not in use in DDR4, DDR1_Vref_DQ = DDR4_CA_ch1, DDR_Vref_CA = DD4_CA_ch0. 13.

undefined



ned undefined undefined 7.2.2.3 **DDR4 DC Specifications**

ndefined und Table 7-18. DDR4 Signal Group DC Specifications

	(intel)	thed undefi	neo -		Electrica	al Specif	fications	
1 UI .		R4 DC Specifications R4 Signal Group DC Specifications			ndefined			
ett.	Symbol	Aefine Parameter	U/U- 4	Core-Proces	ssor Line	Units	Notes ¹	ed u
		4 UNC	Min	Тур	Мах			Letin
	V _{IL}	Input Low Voltage	nedur	_	VREF(INT) - 0.07*VDDQ	V	2, 4, 8, 9, 13	Nor
	VIH UNC	Input High Voltage	VREF(INT) + 0.07*VDDQ	-	_	Ne	3, 4, 8, 9, 13	
	R _{ON_UP/DN(DQ)}	DDR4 Data Buffer pull-up/ down Resistance		Trainable	ed	Ω	11	
ed un	R _{ODT(DQ)}	DDR4 On-die termination equivalent resistance for data signals		Trainable	define	Ω	11	
efine	V _{ODT(DC)}	DDR4 On-die termination DC working point (driver set to receive mode)	0.45*V _{DDQ}	0.5*V _{DDQ}	0.55*V _{DDQ}	V	9	6-
	R _{ON_UP/DN(CK)}	DDR4 Clock Buffer pull-up/ down Resistance	0.8*Typ	26	1.2*Typ	Ω	5, 11	sineu
	R _{ON_UP/DN(CMD)}	DDR4 Command Buffer pull-up/ down Resistance	0.8*Typ	20	1.2*Typ	Ω	11	Inder
	R _{ON_UP/DN(CTL)}	DDR4 Control Buffer pull-up/ down Resistance	0.8*Тур	20	1.2*Typ	Ω	5, 11	
	R _{ON_UP/DN} (DDR_VTT_CNTL)	System Memory Power Gate Control Buffer Pull-Up/ down Resistance	40	_	140	UDIO	-	
lefined ut	ILI	Input Leakage Current (DQ, CK) 0 V 0.2*V _{DDQ} 0.8*V _{DDQ}	_	-od	undefine	mA	-	
	DDR0_VREF_DQ DDR1_VREF_DQ DDR_VREF_CA	VREF output voltage	Trainable	V _{DDQ} /2	Trainable	v	12, 14	ndefined
	DDR_RCOMP[0]	ODT resistance compensation	cineu	·		Ω	6	0.
	DDR_RCOMP[1]	Data resistance compensation	RCOMP value	ues are mem dependent.		Ω	6	
	DDR_RCOMP[2]	Command resistance compensation]	·		Ω	6	
	DDR_RCOMP[2]	Command resistance compensation				Ω	6	-

Notes:

- Unless otherwise noted, all specifications in this table apply to all processor frequencies.
- V_{IL} is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
- 3. $v_{\rm IH}^{\rm T}$ is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
- V_{IH} and V_{IL} may experience excursions above V_{DDO}. However, input signal drivers should comply with the signal quality 4. specifications.

5. This is the pull up/down driver resistance after compensation. Note that BIOS power training may change these values significantly based on margin/power trade-off. See processor I/O Buffer Models for I/V characteristics. DDR_RCOMP resistance should be provided on the system board with ±1% resistors. DDR_RCOMP resistors are to V_{SS}.

- 6. 7. DDR_VREF is defined as $V_{DDQ}/2$ for DDR4 R_{ON} tolerance is preliminary and might be subject to change. The value will be set during the MRC boot training within the specified range.
- 8.
- 9.
- The value will be set during the Mice boot training within the specified range.
 Processor may be damaged if V_{IH} exceeds the maximum voltage for extended periods.
 Final value determined by BIOS power training, values might vary between bytes and/or units.
 VREF values determined by BIOS training, values might vary between units.
 VREF(INT) is a trainable parameter whose value is determined by BIOS for margin optimization.

- DDR0_Vref_DQ Not in use in DDR4, DDR1_Vref_DQ = DDR4_CA_ch1, DDR_Vref_CA = DD4_CA_ch0 14.

ined undefined Datasheet, Volume 1 of 2 -4 undefined

undefinedu



ed undefined undefine 7.2.2.4 **Digital Display Interface (DDI) DC Specifications**

Table 7-19. Digital Display Interface Group DC Specifications (DP/HDMI)

Symbol	Parameter	Min	Тур	Max	Units	Notes ¹
V _{OL}	DDIB_TXC[3:0] Output Low Voltage DDIC_TXC[3:0] Output Low Voltage DDID_TXC[3:0] Output Low Voltage	ed Unde	_	0.25*V _{CCIO}	v	1,2
V _{OH}	DDIB_TXC[3:0] Output High Voltage DDIC_TXC[3:0] Output High Voltage DDID_TXC[3:0] Output High Voltage	0.75*V _{CCIO}	_	_	Vet	1,2
ZTX-DIFF-DC	DC Differential Tx Impedance	80	100	120	Ω	

embedded DisplayPort* (eDP*) DC Specification 7.2.2.5

Table 7-20. embedded DisplayPort* (eDP*) Group DC Specifications

	Symbol	Parameter	Min	Тур	Max	Units
	V _{OL}	eDP_DISP_UTIL Output Low Voltage	-	_	0.1*V _{CCIO}	V
	V _{OH}	eDP_DISP_UTIL Output High Voltage	0.9*Vcc _{IO}	_	. utros	V
	R _{UP}	eDP_DISP_UTIL Internal pull-up	100		<u>o</u> –	Ω
d un	R _{DOWN}	eDP_DISP_UTIL Internal pull-down	100	e4	_	Ω
defined	eDP_RCOMP	eDP resistance compensation	24.75	25	25.25	Ω
der	ZTX-DIFF-DC	DC Differential Tx Impedance	80	100	120	Ω
UI.	Notes: 1. COMP resistan	ice is to VCOMP OUT.	deth		•	

COMP resistance is to VCOMP OUT. 1. 2.

eDP_RCOMP resistor should be provided on the system board.

7.2.2.6 CMOS DC Specifications

Table 7-21. CMOS Signal Group DC Specifications

	Table 7-2	• L. CMOS Signal Group DC S	pecifications			. u	nder.
	Symbol	Parameter	Min	Мах	Units	Notes ¹	
60	V _{IL}	Input Low Voltage	_	Vcc * 0.3	V	2, 5	
stined	V _{IH}	Input High Voltage	Vcc * 0.7	-	V	2, 4, 5	
	V _{OL}	Output Low Voltage	_	Vcc * 0.1	v	2	
	V _{OH}	Output High Voltage	Vcc * 0.9	" ² de.	V	2, 4	194
	R _{ON}	Buffer on Resistance	23	73	Ω	-	Inoc
	I _{LI}	Input Leakage Current		±150	μA	3	

- The Vcc referred to in these specifications refers to instantaneous Vcc levels. For VIN between "0" V and Vcc Measured when the driver is tri-stated. 2
- 3. 4.

 V_{IH} and V_{OH} may experience excursions above Vcc. However, input signal drivers should comply with the signal quality specifications. e------

5. N/A

undefined unde Datasheet, Volume 1 of 2 .re



GTL and OD DC Specifications 7.2.2.7

Table 7-22. GTL Signal Group and Open Drain Signal Group DC Specifications

Symbol	Parameter	Min	CO Max	Units	Notes ¹	5-
V _{IL}	Input Low Voltage (TAP, except PROC_TCK, PROC_TRST#)	- Indet	Vcc * 0.6	V	2, 5, 6	defined
V _{IH}	Input High Voltage (TAP, except PROC_TCK, PROC_TRST#)	Vcc * 0.72	-	V	2, 4, 5, 6	lur.
VIL	Input Low Voltage (PROC_TCK,PROC_TRST#)	_	Vcc * 0.3	V	2, 5, 6	
VIH	Input High Voltage (PROC_TCK,PROC_TRST#)	Vcc * 0.3	—	V	2, 4, 5, 6	
V _{HYSTERESIS}	Hysteresis Voltage	Vcc * 0.2	-	O V	-	
R _{ON}	Buffer on Resistance (TDO)	7	17	Ω	-	
V _{IL}	Input Low Voltage (other GTL)	_	Vcc * 0.6	V	2, 5, 6	
V _{IH}	Input High Voltage (other GTL)	Vcc * 0.72	eo -	V	2, 4, 5, 6	
R _{ON}	Buffer on Resistance (CFG/BPM)	16	24	Ω	-	eine
R _{ON}	Buffer on Resistance (other GTL)	12	28	Ω	-	dell
ILI	Input Leakage Current	e <u>o</u>	±150	μA	3 \lambda	U1.

Unless otherwise noted, all specifications in this table apply to all processor frequencies. The Vcc_{ST} referred to in these specifications refers to instantaneous $Vcc_{ST/IO}$.

1. 2.

3.

For V_{IN} between 0 V and Vcc_{ST}. Measured when the driver is tri-stated. V_{IN} and V_{OH} may experience excursions above Vcc_{ST}. However, input signal drivers should comply with the signal quality specifications. 4.

5. N/A

Those V_{IL}/V_{IH} values are based on ODT disabled (ODT Pull-up not exist). 6.

7.2.2.8 **PECI DC Characteristics**

The PECI interface operates at a nominal voltage set by Vcc_{ST}. The set of DC electrical specifications shown in the following table is used with devices normally operating from a Vcc_{ST} interface supply.

Vcc_{ST} nominal levels will vary between processor families. All PECI devices will operate at the Vcc_{ST} level determined by the processor installed in the system.

Table 7-23. PECI DC Electrical Limits (Sheet 1 of 2)

		ethear Ellines (Sheet I o	-)	0			
undefined Table 7 23.	Symbol	Definition and Conditions	Min	Мах	Units	Notes ¹	
unc	R _{up}	Internal pull up resistance	15	45	Ω	3	adefined
	VIN	Input Voltage Range	-0.15	Vcc _{ST} + 0.15	V	-	defin
	V _{Hysteresis}	Hysteresis	0.15 * Vcc _{ST}	-	V	-	4 UNC
× 1		Input Voltage Low- Edge Threshold Voltage	defin-	0.3 * Vcc _{ST}	V	18tine	
undefined undefined i	V _{IH}	Input Voltage High-Edge Threshold Voltage	0.7 * Vcc _{ST}	_	v	uno <u>-</u>	
Inoc	C _{bus}	Bus Capacitance per Node	N/A	10	pF	-	
	C _{pad}	Pad Capacitance	0.7	1.8	pF	-	
10fill	Ileak000	leakage current @ 0V	—	0.6	mA	-	
unos	Ileak025	leakage current @ 0.25* Vcc _{ST}	—	0.4	mA	-	ed
	Ileak050	leakage current @ 0.50* Vcc _{ST}		0.2	mA	-	Jefil'
120 Ained undefined	undefines	ned undefined l	-defined L			Air	ed und
120		24		C	oatasheet, V	olume 1 of 2	
defin							
1 Une					stine		
stineo		red un		d UP	102		
76.				20			



Table 7-23. PECI DC Electrical Limits (Sheet 2 of 2)

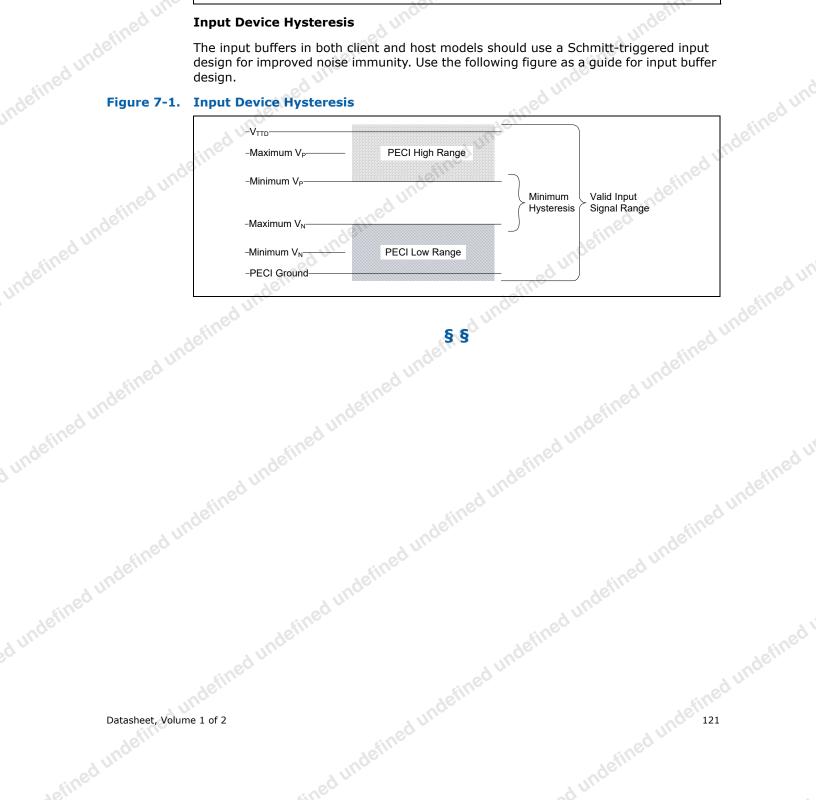
Symbol	Definition and Conditions	Min	Max	Units	Notes ¹
Ileak075	leakage current @ 0.75* Vcc _{ST}	-	0.13	mA	-
Ileak100	leakage current @ Vcc _{ST}	- 18/11	0.10	mA	-
Notes:	•				

 Vcc_{ST} supplies the PECI interface. PECI behavior does not affect Vcc_{ST} min/max specifications. 2. The leakage specification applies to powered devices on the PECI bus 3. The PECI buffer internal pull up resistance measured at 0.75* Vcc_{ST}.

Input Device Hysteresis

The input buffers in both client and host models should use a Schmitt-triggered input design for improved noise immunity. Use the following figure as a guide for input buffer design.





Package Mechanical Specifications

undefined und

(intel) red under

8

undefined undefined un

ndefined und

Package Mechanical Specifications

Package Mechanical Attributes 8.1

The U/U-4 Core/Y Processors use a Flip Chip technology available in a Ball Grid Array (BGA) package. The following table provides an overview of the mechanical attributes of the package.

ndefined un Table 8-1. **Package Mechanical Attributes**

Package Me	echanical Attributes			undef		
Package	Parameter	Y-Processor Line	U- Proces	ssor Line	U-Quad Core Processor Line	d undefined un
fineo		Dual Core GT2	Dual Core GT3+OPC	Dual Core GT2	Quad Core GT2	d unde.
	Package Type	Flip Chip Ball Grid Array	Flip Chip Arr		Flip Chip Ball Grid Array	Nec.
Package	Interconnect	Ball Grid Array (BGA)	Ball Gri (BG		Ball Grid Array (BGA)	
Technology	Lead Free	Yes	Ye	es	Yes	
	Halogenated Flame Retardant Free	Yes	Ye	es unde	Yes	
	Solder Ball Composition	SAC1205	SAC	405	SAC405	2 v
No .	Ball/Pin Count	1515	13	56	1356	fine
ed -	Grid Array Pattern	Balls Anywhere	Balls An	ywhere	Balls Anywhere	d undefined u
Package Configuration	Land Side Capacitors	No	Ye	es	Yes	ed u.
	Die Side Capacitors	No	N	0	No	INO
	Die Configuration	2 Dice Multi-Chip Package (MCP)	3 Dice MCP	2 Dice MCP	2 Dice MCP	
Package	Nominal Package Size	20.5x16.5 mm	42x24	1 mm	42x24 mm	1
Dimensions	Min Ball/Pin pitch	0.4 mm	0.65	mm 🔥	0.65 mm	1

Lundefined undefined ur Package Loading Specifications

Table 8-2.

Package Loa	ding Specifica	0		
Package Loading S		ntions interine		undefined
Maximum Static Normal Load	Limit	Minimum PCB Thickness Assumptions	Notes	
Y/ AML-Y22 Processor Lines	44.5 N (10 lbf)	0.7 mm	1, 2, 3	
U/U- 4 Core Processor Line	67 N (15 lbf)	0.8 mm	1, 2, 3	
sined undefin		ed undefined c		undefined
undell	d undefined unde	Datasheet,	, Volume 1 of 2	
	Maximum Static Normal Load Y/ AML-Y22 Processor Lines U/U- 4 Core	Normal Load Limit Y/ AML-Y22 44.5 N (10 lbf) U/U- 4 Core 67 N (15 lbf)	Maximum Static Normal Load Limit Minimum PCB Thickness Assumptions Y/ AML-Y22 Processor Lines 44.5 N (10 lbf) 0.7 mm U/U- 4 Core Processor Line 67 N (15 lbf) 0.8 mm	Maximum Static Normal LoadLimitMinimum PCB Thickness AssumptionsNotesY/ AML-Y22 Processor Lines44.5 N (10 lbf)0.7 mm1, 2, 3U/U- 4 Core Processor Line67 N (15 lbf)0.8 mm1, 2, 3

Package Mechanical Specifications



Table 8-2. Package Loading Specifications

 Notes: The thermal solution attach mechanism should not induce continuous stress to the package. It may only apply a uniform load to the die to maintain a thermal interface. This specification applies to the uniform compressive load in the direction perpendicular to the dies' top surface. Load should be centered on processor die center. This specification is based on limited testing for design characterization. This load limit assumes the use of a backing plate. 		Minimum PCB Thickness Assumptions Notes	Limit	aximum Static Normal Load
	119	l interface. load in the direction perpendicular to the dies' top inter.	e die to maintain a ther o the uniform compress ntered on processor die on limited testing for de	The thermal solution attact apply a uniform load to the This specification applies to surface. Load should be ce This specification is based

- surface. Load should be centered on processor die center. This specification is based on limited testing for design characterization. This load limit assumes the use of a backing plate.
- 3. 4.

undefined under 8.3

Package Storage Specifications

Table 8-3. Package Storage Specifications

Table 8-3.	Package Storage	Specifications	Indetin			
	Parameter	Description	Min	Max	Notes	6
60.	TABSOLUTE STORAGE	The non-operating device storage temperature. Damage (latent or otherwise) may occur when subjected to this temperature for any length of time in Intel Original sealed moisture barrier bagand / or box.	-25 °C	125 °C	1, 2, 3	ndefine
defined un	TSUSTAINED STORAGE	The ambient storage temperature limit (in shipping media) for the sustained period of time as specified below in Intel Original sealed moisture barrier bagand / or box.	-5 °C	40 °C	1, 2, 3	
ined une	RH _{SUSTAINED} STORAGE	The maximum device storage relative humidity for the sustained period of time as specified below in Intel Original sealed moisture barrier bagand / or box	60%	@ 24 °C	1, 2, 3	
undefined unr	TIMESUSTAINED STORAGE	Maximum time: associated with customer shelf life in Intel Original sealed moisture barrier bag and / or box	NA	Moisture Sensitive Devices: 60 months from bag seal date; Non- moisture sensitive devices: 60 months from lot date	1, 2, 3	undefine

Notes:

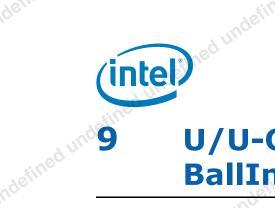
Specified temperatures are based on data collected. Exceptions for surface mount re-flow are specified 2. by applicable JEDEC J-STD-020 and MAS documents. The JEDEC, J-STD-020 moisture level rating and associated handling practices apply to all moisture sensitive de-vices removed from the moisture barrier bag.

3. . Cc Post board attach storage temperature limits are not specified for non-Intel branded boards. Consult your board manufacturer for storage specifications. undefined undefined undefined

ed undefined undefined un

undefinedu

defined ur U/U-Quad Core/YProcessor BallInformation



g

U/U-Quad Core/YProcessor **BallInformation**

U-Processor and U-Quad Core Processor Ball 9.1 Information

, ie , of the , of the undefined und The U-Processors and U-Quad Core Processors are available in the BGA package undermed underme (BGA1356), Figure 9-1 through Figure 9-6 provide a top view of the Ball map.

126 The survey interined indefined i

(intel) defined un

	71	70	69	68	67	66	65 G	64	63	62	61	60 60	59 (Up	58	Left, 57	56	mns	5 4	5 3	52	51	50	49	48	
ndefine		VSS	RSVD_T P	RSVD_T P	VSS	VccGTx	DDR0_ DQ[16] / DDR0_ DQ[32]	VSS	DDR0_ DQ[23] / DDR0_ DQ[39]		DDR0_ DQ[28] / DDR0_ DQ[44]	VSS	DDR0_ DQ[26] / DDR0_ DQ[42]		VccGTx	DDR0_C KE[1]	VSS	DDR0_ MA[9]/ DDR0_C AA[1]/ DDR0_ MA[9] DDR0_		DDR0_ MA[4]	VDDQ	DDR0_ MA[1] / DDR0_C AB[8]/ DDR0_ MA[1]	-	DDR1_ MA[8]/ DDR1_C AA[3]/ DDR1_ MA[8]	96
ВА	VSS	RSVD_T P		RSVD_T P	DDR1_V REF_DQ	vss	DDR0_ DQ[20] / DDR0_ DQ[36]	DDR0_ DQSN[2]/ DDR0_ DQSN[4]	DDR0_ DQ[22] / DDR0_ DQ[38]	VSS	DDR0_ DQ[24] / DDR0_ DQ[40]	DDR0_ DQSP[3]/ DDR0_ DQSP[5]	DDR0 DQ[30] / DDR0_ DQ[46]	n o C	VSS	DDR0_C KE[0]	DDR0_ MA[15] / DDR0_C AA[8]/ DDR0_A CT#	MA[11] / DDR0_C AA[7]/ DDR0_ MA[11] DDR0	VSS	DDR0_ MA[6]/ DDR0_C AA[2]/ DDR0_ MA[6]	AA[0] / DDR0_ MA[5]	MA[3]	VSS	DDR1_ MA[6] / DDR1_C AA[2] / DDR1_ MA[6]	
AY	VSS		ned	DDR0_V REF_DQ	DDR_VR EF_CA	VSS	DDR0_ DQ[21] / DDR0_ DQ[37]	DDR0_ DQSP[2]/ DDR0_ DQSP[4]	DDR0_ DQ[19] / DDR0_ DQ[35]		DDR0_ DQ[29] / DDR0_ DQ[45]	DDR0 DQSN[3]/ DDR0 DQSN[5]	DDR0_ DQ[31] / DDR0_ DQ[47]			DDR0_C KE[3]	DDR0_B A[2]7 DDR0_C AA[5]/ DDR0_B G[0]	MA[14] DDR0_C AA[9]/ DDR0_B G[1]	, U	DDR0_ MA[8]7 DDR0_C AA[3]7 DDR0_ MA[8]	DDR0_ MA[2]/ DDR0_0 AB[5]/ DDR0_ MA[2]	DDR0_ MA[0]7 DDR0_C AB[9]/ DDR0_ MA[0]		DDR1_ MA[5]/ DDR1_C AA[0]/ DDR1_ MA[5]	
AW	RSVD_T P VSS	RSVD_T P VSS	RSVD VSS	RSVD VSS	DDR_VT T_CNTL	VSS	DDR0 DQ[17] / DDR0_ DQ[33]	VSS	DDR0 DQ[18] / DDR0 DQ[34]	Vss	DDR0_ DQ[25] / DDR0_ DQ[41]	VSS	DDR0 DQ[27] / DDR0_ DQ[43]		VSS	DDR0_C KE[2]	VSS	DDR0_ MA[12] / DDR0_C AA[6] / DDR0_ MA[12]		DDR0_ MA[7]7 DDR0_C AA[4] / DDR0_ MA[7]	VSS	DDR0_A LERT#	VSS	RSVD	5
JUNGELA	DDR0	DDR0	DDR0_ DQ[15]	DDR0		DDR1_ DQ[17] / DDR0_ DQ[49]	DDR1_ DQ[23] / DDR0_ DQ[55]		VccGTx		DDR1_ DQ[25] / DDR0_ DQ[57]	DDR1_ DQ[31] / DDR0_ DQ[63]		VccGTx	def	RSVD	DDR0_C KN[1]		DDR0_C KN[0]	DDR0_E A[0] / DDR0_C AB[4]/ DDR0_E A[0]	3	DDR0_R AS# / DDR0_C AB[3]/ DDR0_ MA[16]	efin	DDR0_C AS#/ DDR0_C AB[1]/ DDR0_ MA[15]	
AT	VSS	DDR0_ DQSP[1]	DDR0_ DQSN[1]	vss	defil	DDR1 DQ[16] / DDR0 DQ[48]	DDR1_ DQ[22] / DDR0_ DQ[54]		VSS		DDR1_ DQ[24] / DDR0_ DQ[56]	DDR1_ DQ[30] / DDR0_ DQ[62]	644	vss		VSS	DDR0_C KP[1]		DDR0_C KP[0]	DDR0_F	Iner	DDR0_ MA[10] / DDR0_C AB[7]/ DDR0_ MA[10]		DDR0_E A[1] / DDR0_C AB[6]/ DDR0_E A[1]	-
AR	DDR0_ DQ[12]	DDR0_ DQ[8]	DDR0_ DQ[13]	DDR0_ DQ[9]		DQSN[2]/ DDR0_ DQSN[6] DDR1_ DOR1_	DQSP[2]/ DDR0 DQSP[6] DDR1_		VSS	1001	DQSN[3]/ DDR0 DQSN[7] DDR1_ DDR1_	DQSP[3]/ DDR0_ DQSP[7] DDR1_ DO[26]		VSS		ZVM#	VSS		VSS	VSS DDR1_E A[2]7 DDR1_C		VSS DDR1_ MA[9]7		VSS DDR1_ MA[7]/ DDR1_C	,
undefi	DDB0	VSS DDR0	DDR0	VSS DDR0_		DQ[21] DDR0_ DQ[53] DDR1_ DQ[20]	DQ[18] / DDR0_ DQ[50] DDR1_ DQ[19]	 Stine	vss		DQ[29] / DDR0_ DQ[61] DDR1_ DQ[28]	DQ[26] / DDR0_ DQ[58] DDR1_ DQ[27]		VSS		MSM#	DDR1_C KE[1] DDR1_C		DDR1_C KE[3] DDR1_ MA[15] /	AA[5]/ DDR1_E G[0] DDR1_ MA[14] /		DDR1_C AA[1]/ DDR1 MA[9] DDR1_ MA[12] /		AA[4] / DDR1 MA[7] DDR1 MA[11]	
AN AN	DQ[7]	DQ[6] DDR0 DQSN[0]	DQ[3] DDR0 DQSP[0]	DQ[2]	. Jet	DDR0_ DQ[52]	DDR0_ DQ[51]		VSS		DDR0_ DQ[60]	DDR0_ DQ[59] VSS		VSS VccGTx	nëc 	KE[0]	VSS		DDŔ1_C AA[8]/ DDR1_A CT#	DDŔ1_C AA[9]/ DDR1_E G[1] VccGTx	3	DDŔ1_C AA[6]/ DDR1_ MA[12] VccGTx	det l	DDŔ1_C AA[7]/ DDR1 MA[11] VccGTx	
AL	DDR0_ DQ[0]	DDR0 DQ[4] VccGTx	DDR0 DQ[5] VSS	DDR0 DQ[1] VSS	DDR1_ DQ[6] / DDR0_ DQ[22]	VSS DDR1_ DQ[7]/ DDR0_ DQ[23]	VSS DDR1_ DQ[2]7 DDR0_ DQ[18]	VSS DDR1_ DQ[3]/ DDR0_ DQ[19]	VCCEOP IO_SEN SE	 VCCGTx _SENSE	VSSGTx _SENSE	VccGTx VccGTx		VSS VccGTx		VccGTx VccGTx	VSS VccGTx		VccGTx VccGTx	VSS VccGTx		VccGTx VccGTx		VSS VccGTx	
EA HA	DDR1_ DQ[10]	DDR1_ DQ[14]	DDR1_ DQ[15]	DDR1_ DQ[11]	VSS	DDR1_ DQSN[0]/ DDR0	DDR1_ DQSP[0]/ DDR0	VSS	VSS	VSSEOP IO_SEN SE							 2{1}	deri							
a unos		DDR1_ DQSP[1]/ DDR0	DDR0 DQ[31] DDR1 DQSN[1]/ DDR0 DQSN[3	DDŔ0 DQ[27]		DQSN[2				VCCEOP IO					und	eine							0.96 ³	ined	
AF	DDR1_ DQ[12] / DDR0_ DQ[28]	J DQ[8]7 DDR0_ DQ[24]		8		DDR1_ DQ[4]7 DDR0_ DQ[20]	DDR1_ DQ[0]7 DDR0_ DQ[16]		VSS VSSOP-			 	defi	<u></u>							etif	e <u>0</u>			-
AE AD AC AB	VCCGT	N/A VCCGT	VSS VCCGT	VSS VCCGT	VSS VCCGT	VSS VCCGT	VSS VCCGT	VSS VCCGT	VCCOP-	VCCEOP IO VSS								 		 					-
ad unde	TITE							defi	ned	Peccorc		1	Indef			Jefin	edu	L	1	1	1	1	 کد	afine	, 6 /
					und	stine							de	ined							in the second	ned	nuo.		
	etine	Da	atashe	et, Volu	ume 1	of 2					lefin	ed l	71.						fine	d un		127			
	etine	ġ,						ć	ned	Jun							.6	unde	5						

U/U-Quad Core/YProcessor BallInformation Figure 9-1. U/U-Quad Core Processor Ball Map (Upper Left, Columns 71-48)



		47	46	45	9-2 .	43	42	41	40	39	38	37	311 M 36	ар (ч 35	34	33	32	31	30	29	28	27	26	25	24	
ndef	вв	VDDQ	DDR1_ MA[3]		DDR1_ BA[0] / DDR1_ CAB[4] / DDR1_ BA[0]	VSS	DDR1_ CS#[0]	VDDQ	efin	DDR0 DQ[36] / DDR1 DQ[4]	VSS	DDR0_ DQ[39] / DDR1_ DQ[7]		DDR0_ DQ[44] / DDR1_ DQ[12]		DDR0_ DQ[47] / DDR1_ DQ[15]		DDR0 DQ[52] / DDR1_ DQ[36]	VSS	DDR0 DQ[55] / DDR1_ DQ[39]		DDR0_ DQ[60] / DDR1_ DQ[44]	V 22	DDR0_ DQ[63] / DDR1_ DQ[47]		red unde
	BA	DDR1_ MA[4]	DDR1_ MA[0]7 DDR1_ CAB[9] DDR1_ MA[0]	VSS	DDR1 BA[1]7 DDR1_ CAB[6] DDR1_ BA[1]	DDR1_ MA[13] DDR1_ CAB[0] DDR1_ MA[13]	DDR1_ ODT[0]	VSS			DDR0_ DQSN[4] / DDR1_ DQSN[0]	DDR0_ DQ[38] / DDR1_ DQ[6]	VSS	DDR0 DQ[45] / DDR1_ DQ[13]	DDR0_ DQSP[5]/ DDR1_ DQSP[1]	DDR0_ DQ[46] / DDR1_ DQ[14]	VSS	DDR0 DQ[53] / DDR1_ DQ[37]	DDR0_ DQSN[6] / DDR1_ DQSN[4]	DDR0 DQ[54] / DDR1_ DQ[38]	VSS	DDR0_ DQ[61] / DDR1_ DQ[45]		DDR0_ DQ[62] / DDR1_ DQ[46]	Je _l	
	AY	DDR1_ MA[2]7 DDR1_ CAB[5] / DDR1_ MA[2]	DDR1_ MA[1]7 DDR1_ CAB[8] / DDR1_ MA[1]	tine		DDR1_ CAS#/ DDR1_ CAB[1] / DDR1_ MA[15]	DDR1_ CS#[1]			DDR0_ DQ[32] / DDR1_ DQ[0]	DDR0_ DQSP[4]/ DDR1_ DQSP[0]	DDR0_ DQ[34] / DDR1_ DQ[2]	<u>d u</u>	DDR0_ DQ[40] / DDR1_ DQ[8]	DDR0_ DQSN[5] / DDR1_ DQSN[1]	DDR0_ DQ[42] / DDR1_ DQ[10]		DDR0_ DQ[48] / DDR1_ DQ[32]	DDR0_ DQSP[6]/ DDR1_ DQSP[4]	DDR0_ DQ[50] / DDR1_ DQ[34]	0	DDR0_ DQ[56] DDR1_ DQ[40]		DDR0_ DQ[58] / DDR1_ DQ[42]		
nde	AW	vss	DDR1_ MA[10] DDR1_ CAB[7] DDR1_ MA[10]	VSS	DDR1_ RAS# / DDR1_ CAB[3] / DDR1_ MA[16]		DDR1_ ODT[1]	VSS	- Fil	DDR0_ DQ[33] / DDR1_ DQ[1]	VSS	DDR0_ DQ[35] / DDR1_ DQ[3]	VSS	DDR0_ DQ[41] / DDR1_ DQ[9]		DDR0_ DQ[43] / DDR1_ DQ[11]		DDR0_ DQ[49] / DDR1_ DQ[33]	VSS	DDR0 DQ[51] / DDR1_ DQ[35]	VSS	DDR0 DQ[57] / DDR1 DQ[41]	•33	DDR0_ DQ[59] / DDR1_ DQ[43]		ned und
71,	AV AU		DDR0_ MA[13] / DDR0_ CAB[0] / DDR0_ MA[13]	DDR0_ CS#[0]		DDR0_ CS#[1]	VDDQ	un	DDR1_ DQ[32] / DDR1_ DQ[16]		VSS	DDR1_ DQ[35] / DDR1_ DQ[19]		VDDQ	 	DDR1_ DQ[41] DDR1_ DQ[25]			DDR1_ DQ[42] / DDR1_ DQ[26]		VDDQ	DDR1_ DQ[48]		DDR1_ DQ[51]	<u>9</u> e	iuer.
	AT		DDR0_ WE#/	DDR0_ ODT[0]	<u>, d</u>	DDR0_ ODT[1]	VSS		DDR1 DQ[33] / DDR1_ DQ[17]		DDR1_ DQSN[4] / DDR1_ DQSN[2]	DDR1_ DQ[34] / DDR1_ DQ[18]	eð	Vss		DDR1_ DQ[40] / DDR1_ DQ[24]	DODI		DDR1 DQ[43] / DDR1_ DQ[27]		vss	DDR1 DQ[49]		DDR1 DQ[50]		-
2	AR	ned	VSS	VSS		VSS	VSS		DDR1 DQ[36] / DDR1 DQ[20] DDR1 DQ[37]	ned	DDR1_ DQSP[4]/ DDR1_ DQSP[2]	DDR1_ DQ[39] / DDR1_ DQ[23] DDR1_ DQ[38]		VSS		DDR1_ DQ[44] / DDR1_ DQ[28] DDR1_ DQ[45]	DDD1		DDR1_ DQ[46] / DDR1_ DQ[30] DDR1_ DQ[47]	<u>lefi</u> r	vss	DDR1_ DQSP[6]		DDR1_ DQSN[6]		nu ,
UNU	AP AN AM AL		DDR1_ CKP[1] DDR1_ CKN[1] VSS VccGTx	DDR1_ CKP[0] DDR1_ CKN[0] VSS VSS		DDR1_ PAR DDR1_ ALERT# VSS VccGTx	VSS VSS VCCIO VCCIO	<u></u>	DDR1_ DQ[21] VSS VDDQC VCC		VSS VSS VCC VSS	DDR1_ DQ[22] VSS VCC		VSS VSS VCC VSS		VCC	VSS VSS VCC VSS		DDR1 DQ[31] VSS VCCIO VCCIO		VSS VSS VCCIO VSS	DDR1_ DQ[52] DDR1_ DQ[53] VSS RSVD		DDR1_ DQ[55] DDR1_ DQ[54] VSS RSVD	 5.00	ined un
	AK AJ AH AG AF AE	 	VccGTx	VccGTx 		VccGTx	VccGTx	 	VCC 	 	VCC	VCC 	 	VCC 		VCC 	RSVD 	 	VCCIO 	 	VCCIO 	VSS	 	VCCSA	 	
	AD AC AB	ine									9 20								 		6]
d un								ed l	nde	ine						2	undf	stine								efined u
					~ed	und	efill							un	defil								defi	ned		
J UN			d ur	defi							20									nde	tine	ġn,				
ed ut	nde							-0	und	Stin							ind	efin	ed v							terfined I
			12	3		d un	defi								def	ined				Data	asheet	Volur	ne 1 c	ined	Un	
			م م	nde	ine							Inde	stine			ned					stin	., volu		,, <i>L</i>		defined u
		Sin	6							ci (ed								6	JUL						

ed undefined undefined Figure 9-2. U/U-Quad Core Processor Ball Map (Upper Middle, Columns 47-24)



		23	22	21 21	20	19	18	17	16	15	14	13	12 12	<u></u> 11	10	9	8	67	6	5	4	3	2	1	_
ndefil	вв	VDDQ	HDA_SD 07 I2S0_TX D		DSW_P WROK		VSS	GPD9 / SLP_WL AN#	d	WAKE#	VCCRTC	GPP_A3 /LAD2/ ESPI_IO 2		GPP_A7 / PIRQA#	DCPRTC	GPP_A1 6 / SD_1P8 _SEL		GPP_A2 0 / ISH_GP 2	VSS	TP4	RSVD	TP2	RSVD		nde
nos	BA	VSS	HDA_SY NC / I2S0_SF RM	HDA_SD IO/ I2S0_R XD	PCH_PW ROK		vss	GPD8 / SUSCLK	GPD5 / SLP_S4 #	GPD3 / PWRBTN #	VSS	GPP_A2 / LAD1 / ESPI_IO 1	GPP_A5 / LFRAME # / ESPI_CS #	GPP_A1 47 SUS_ST AT#/ ESPI_RE SET#	VSS	GPP_A1 7 / SD_PW R_EN# / ISH_GP 7	1		VSS	GPP_B3 / CPU_GP 2	RSVD	RSVD	VSS	VSS	
	AY		HDA_BL K / I2S0_S CLK	HDA_SD I1 / I2S1_R XD	I2S1_SF RM	įΩ		RSMRST #	GPD10/ SLP_S5 #	GPD1 / ACPRES ENT		GPP_A1 /LAD0/ ESPI_IO 0	GPP_A4 / LAD3 / ESPI_IO 3	GPP_A6 / SERIRQ		GPP_A1 07 CLKOUT _LPC1	8 / ISH_GP 0	GPP_A2 2 / ISH_GP 4		GPP_B4 CPU_GP 3	TP1	RSVD	RSVD	RSVD	
	AW	VSS	HDA_RS T# / I2S1_S CLK	VSS	I2S1_TX D		VSS	GPD11/ LANPHY PC	VSS	SLP_LA N#	VSS	GPP_A0 / RCIN#	VSS	GPP_A8 / CLKRUN #	VCC	GPP_A9 / CLKOUT _LPC0 / ESPI_CL	VSS	GPP_A2 3 / ISH_GP 5	VSS	GPP_B1 47 SPKR	N/A	SPI0_MI SO	SPIO_IC	RSVD	
	AV		<u> 02</u>													К			<u>e</u>			SPI0_M OSI	SPI0_CI K	VSS	
ć	AU	VDDQ	DDR1_D Q[57]	DDR1_D Q[58]	VSS		DDR_RC OMP[2]		PCH_OP IRCOMP	vss		GPD0 / BATLOW #		GPP_A1 1 /PME#			GPP_B9 / SRCCLK REQ4#	0 / SRCCLK REQ5#		TP5	SPI0_IC	SPI0_C S0#	SPI0_C S1#	SPI0_C S2#	5
Indei	AT	VSS	DDR1_D Q[56]	DDR1_D Q[59]	VSS		DDR_RC OMP[1]	deriv	PROC_P OPIRCO MP	GPD7 / RSVD		DRAM_R ESET#		GPP_B1 27 SLP_S0 #	GPP_B8 / SRCCLK REQ3#	sin ^e	GPP_B7 / SRCCLK REQ2#	GPP_B6 / SRCCLK REQ1#		TP6	VSS		VSS	EMMC_R COMP	Un
	AR	VSS	DDR1_D QSN[7]	DDR1_D QSP[7]	VSS	sine	DDR_RC OMP[0]		VSS	VSS		GPP_A1 3/ SUSWA RN#/ SUSPW RDNACK		VSS	GPP_B5 / SRCCLK REQ0#		VSS	GPP_B1 87 GSPI0_ MOSI		VSS			1981		
	AP	VSS	DDR1_D Q[61]	DDR1_D Q[62]	Vss		VSS		INTRUD ER#	GPD4 / SLP_S3 #		Sx_EX- IT_HOL DOFF#/ GPP_A1 27 BM_BUS Y#/ ISH_GP 6	def	GPP_A1 5 / SUSACK #	VSS		GPP_B1 7/ GSPI0_ MISO	GPP_B1 67 GSPI0_ CLK		GPP_B2 17 GSPI1_ MISO	GPP_F1 27 EMMC_C MD	GPP_F1 57 EMMC_ DATA2	GPP_F1 37 EMMC_ DATA0	4/	
	AN	VSS	DDR1_D Q[60]	DDR1_D Q[63]	VSS		SRTCRS T#		GPD6 / SLP_A#	SLP_SU S#	e <u></u>	GPP_B1 / CORE_V ID1		GPP_B0 / CORE_V ID0	3/		GPP_B1 5 / GSPI0_ CS#	GPP_B2 0/ GSPI1_ CLK	<u>lue</u>	GPP_B2 2/ GSPI1_ MOSI		GPP_F1 67 EMMC_ DATA3	GPP_F1 8 / EMMC_ DATA5	7/	
unde	АМ	VCCIO_ SENSE	VSSIO_ SENSE	VSS	RTCX2		RTCX1	-7e	RTCRST #	GPD2 / LAN_WA KE#		VSS		GPP_B2 / VRALER T#	GPP_B1 17 EXT_P- WR_GAT E#		VSS	GPP_B2 3/ SML1AL ERT#/ PCHHOT #		GPP_B1 9/ GSPI1_ CS#	GPP_F1 97 EMMC_ DATA6	GPP_F2		GPP_F2	Un
	AL	VCCPLL _OC						VCCRT-		 VCCPGP		 RSVD_T	 RSVD_T		 GPP_F3	GPP_F2		 GPP_F1	 GPP_F0		VSS		VSS	DCPDS W_1p0	
	AK AJ	VCCSA	VSS	VSS VCCPRI M_3p3	VCCPRI M_1p0	VCCRTC VCCHDA	VSS	CPRIM_ 3p3 VCCDS W_3p3	VSS	VCCFGF PA VSS		P	P	VSS	12S2_R XD	12S2_ТХ D	VSS	12S2_SF RM	12S2_S CLK		VSS	USB2P_	USB2P_ 5	USB2N_ 5	
	АН			M_3p3	<u> </u>							VSS	GPP_F7 / I2C3_S	GPP_F6 / I2C3_S	GPP_F5 / I2C2_S	/ 12C2 S	USB2P_ 10	USB2N_ 10	VSS		<u>9e.</u>	USB2N_	USB2P_ 7	USB2N_ 7	
	AG		nde	VSS	VSS	VSS	VSS	VSS	VSS	VCCPGP PB	1 total	<u> </u>	CL	DA	CL	DA			<u></u> e	o	USB2_V BUSSEN SE	USB2_I D	USB2P_ 9	USB2N_ 9	
	AF	ed		VCCSRA M_1P0	VCCSRA M_1P0	VCCPRI M_CORE	VCCPRI M_CORE	VSS	VCCPGP PF	vss		GPP_F2	GPP_F9 / I2C4_S CL	GPP_F8 / I2C4_S DA	VSS	USB2P_ 8	USB2N_ 8	USB2P_ 6	USB2N_ 6		VSS		VSS	VSS	
a und	AE			VSS	VSS	VSS	VCCDS W_3p3	VCCDS W_3p3	VSS	VCCPGP PG		VSS	 GPP_F1 1/ I2C5_S CL / ISH_I2C	 GPP_F1 0/ I2C5_S DA/ ISH_I2C 2_SDA	USB2P_ 4	USB2N_ 4	VSS	USB2P_ 2	USB2N_ 2		 GPP_C2 37 UART2_ CTS#	 GPP_C2 2 / UART2_ RTS#	 GPP_C2 17 UART2_ TXD	 2 GPP_C2 07 UART2_ RXD	0 ^U
	AC				 10 - 10	defi	<u></u>							Sitte	<u>, , , , , , , , , , , , , , , , , , , </u>							GPP_C1 47 UART1_ RTS#7 ISH_UA RT1_RT S#	GPP_C1 37 UART1_ TXD / ISH_UA RT1_TX D	GPP_C1 27 UART1_ RXD / ISH_UA RT1_RX D	-
	AB		bn.	VSS	VCCPRI M_1P0	VCCPRI M_1P0	VSS	VCCPRI M_1p0	VSS	VSS	201	GPP_G1 / SD_DAT A0	GPP_G2 / SD_DAT A1	/	USB2P_	USB2N_	VSS	SD_RCO	USB2_C OMP	ed u	GPP_C1 5/ UART1_ CTS#/ ISH_UA RT1_CT S#	GPP_C1	GPP_C9 / UART0_ TXD		
ed un	def	Ined	<u>.</u>				ed	und	efin	ed ul		SD /DAT		I	20	nde	ined	und	0					defin	ed l
			Data	asheet,	, Volum	nde ¹ e 1 of	2						uni	Jefin						ed l	Inde	129	9.0.		
		tined	Jun								nde							n,	defil						
		11.							6.0	6								9							

U/U-Quad Core/YProcessor BallInformation Figure 9-3. U/U-Quad Core Processor Ball Map (Upper Right, Columns 23-1)



'dell'				te			ndef	INe							defi	ne ^O Quad (Colu							713	led l	71
			<u>_</u>											d un	11/11-	Quad (ore /	VProce	assar l	RallTni	format	tion			
				le									Stille		0,0	Quuu V				nde	ine	lion			
											ned	0							- d ¹	noe					
	71	70	gure 69	9-4.	67	U-Qi	65 65	64	63	esso 62	61 61	60 60	59 (Lo	58	57	Colu 56	mns 55	71-4	53	52	51	50	49	48	_
AA Y	VCCGT	VCCGT	VCCGT	VSS	VCCGT	VCCGT	VSS	VCCGT	VCCGT	VCCG1							J ²								70
w	VCCGT			VCCGT		VCCGT	VCCGT	VCCGT							50	<u> </u>								<u>60</u>	-
v u	 VCCGT	VSS	 VSS	 VCCGT	 VSS	VSS	 VCCGT	 VSS	 VSS	VCCOF C				50									90		-
т										VCCGT			<u>e</u>								11:00	0			-
R	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT			VCCGT	VCCGT	 VCCOF	2	11								und'					
P N	 VCCGT	VCCGT	VCCGT	VSS	 VCCGT	 VCCGT	VSS	 VCCGT	 VCCGT	C															-
м	<u>65</u>								<u></u>	VCCGT							20	0							
лидег	VCCGT VSS	VCCGT	VCCGT	VCCGT		VCCGT	VCCGT VSS	VCCGT VSS	VCCGT	VCCGT	 VSS	 VCCGT		 VCCGT		VCCGT	VCCGT		 VCCGT	 VCCGT		 VCCGT		 VCCGT	
J	RSVD	VCCGT _SENS E	VSSGT _SENS E	RSVD		-ed	· · · · ·					VCCGT		VCCGT	7 <u>00,</u>	VCCGT	VCCGT		VCCGT	VCCGT		VCCGT	<u>, 06</u>	VCCGT	
н	VSS	CFG[1 2]	CFG[1 4]		9e	OPCE_ RCOM P	OPC_R		VCC_0 PC_1P 8				-41	<u></u>								<u>.0</u>			
G	CFG[1 3]	CFG[1 5]	CFG[9]	CFG[1 1]		VSS	VSS		VSS		VCC_C PC_1P	VSS		VSS		DDI1_ TXP[3]	VSS		DDI1_ TXP[2]	VSS	<u>e</u>	DDI1_ AUXN		VSS	
F	CFG[8]	CFG[1 0]	<u>87.</u>	VSS		CFG[1 9]	VSS		CFG[1 7]		RSVD	RSVD		DDI1_ TXP[1]		DDI1 TXN[3	DDI1_ TXP[0]		DDI1 TXN[2	RSVD		DDI1_ AUXP		DDI2_ AUXP	
E	VSS	CFG[4]		CFG[0]		CFG[1 8]	VSS		CFG[1 6]	100	RSVD	CFG_R COMP		DDI1 TXN[1 1		VSS	DDI1 TXN[0 1	19 <u>6</u>	VSS	eDP_R COMP		VSS		DDI2_ AUXN	f
0 D	RSVD		VSS	CFG[6]	CFG[3]	VSS	CFG[2]	VIDSO UT	CATER R#	VSS	PROC_ PREQ #	PROC_ TDI	PCH_J TAG_T DI	VSS		PROC_ PRDY#	BPM#[1]	RSVD	VSS	DDI2_ TXP[1]	DDI2_ TXN[3]	DDI2_ TXP[0]		VSS	6
с	RSVD	RSVD		CFG[5]	CFG[7]		PROC HOT#	PROC_ SELEC T#	THER MTRIP #		PCH_T RST#	PROC_ TMS	PCH_J TAG_T MS	·	<u></u> d	BPM#[3]	BPM#[0]	RSVD		DDI2_ TXN[1]	DDI2_ TXP[3]	DDI2 TXN[0]		Ω_{ij}	
В	VSS	RSVD	RSVD		CFG[1]	VSS	VCCST _PWR _GD		VIDAL ERT#	VSS	PROC_ TCK		PROC_ TRST#	VSS		PCH_J TAG_T CK		BPM#[2]	VSS	EDP_D ISP_U TIL		DDI2_ TXP[2]	<u>76.</u>	VSS	
А		VSS	RSVD	PROCP WRGD	VSS	VCCGT	SKTOC C#		VIDSC K	VCCGT	PROC_ TDO		JTAGX	VCCGT		PCH_J TAG_T DO		PECI	VCCGT	RSVD	10 CON	DDI2_ TXN[2]		VCCGT	
			1911 192	Ver							0.5	ed								d ur					-
		d un								nn'									sine						
A Junde	sine																.60	JULE							
JUNC							. J	19e,								defit									
															d ur							2	und	6.	
					und	6								fine							Ś				
												ed'								ال	Uge				
		ى ،																							
										9 UN							~	uno							
, und								de								, est	INEC								
							ed '), ·							20	noc								9etr	
						defin								etine											
		13	0		5.01								uno			ndefi		Da	atashe	et, Volu	ume 1	of 2			
												INer								ed)					
		ed l								, U	00-							n.							
	16/11	*							nia	3								90.							

led underine U/U-Quad Core/YProcessor BallInformation une



47ndefined 44 43 42 41 40 39 38 37 36 35 34 33 32 31 30 29 28 27 26 25 24 nde Y ------------------------0 --U --------------------44 -----------------------------------<u>.</u> ------------------------------Т ---------------------R ----------------÷--- 19 ----Ρ ------------64 -----------------------------علايها ------------------------22 --------27 -----------------------Ν ----------------------------end ---Μ --1 ------------------------ 25 -------------------------1 VCCS A RSVD RSVD Κ ------VCC VCC ---VCC --vcc VCC <u>___</u> VCC ---VCC RSVD ----------VCCSA --vss vss J ---------VCC ----VCC --vss ---VCC VSS ---VCC сf VSS VCCSA ---VSS ----Н --G ----RSVD VCC VCC ---VC VCC ----VCC ---VC VCC ---V ---CCSA VCCSA /CCSA ---PCIE1 DP_A PCIE10 _RXN F VSS VSS RSVD -------------------VSS ---------/ SATA2 _RXP PCIE1 PCIE11_ RXN / SATA1B _RXN PCIE11_ RXP / SATA1B _RXP XCLK BIASR EF 2_RXM EDP_A UXN PCIE10 _RXP XTAL2 4_IN XTAL2 4_OUT VSS_S ENSE VCC_S ENSE Е ---_ _ . ------------SATA2 _RXN PCIE11 _TXN / SATA1B _TXN CSI2_D P9 EDP_T XN[1] CSI2 DP5 CSI2 CLKP1 CSI2_D P11 <u>.</u>... e vss VSS VSS VSS VSS VSS D PCIE11 _TXP / SATA1B _TXP CSI2_D N9 EDP_1 XP[1] CSI2 DN4 EDP_T XN[0] EDP_ XP[0] CSI2_D N11 --vss С -------------------PCIE12 _TXP / SATA2_ TXP EDP_1 XP[3] CSI2_D P10 EDP_1 XP[2] --vss ---------vss ---В --undefi A undefined undefined undefined undefined undefined undefined humen not under med PCIE12 _TXN / SATA2_ TXN EDP_T XN[3] EDP_T XN[2] CSI2_ CLKP3 CSI2_D N10 6. --vcc --vcc ------vcc vcc ---......

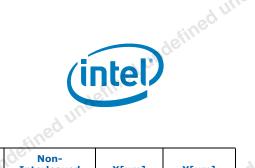
Jed undefined underined U/U-Quad Core Processor Ball Map (Lower Middle, Columns 47-24) Figure 9-5.

Datasheet, Volume 1 of 2 ne undefi



qe,				in				defi	IUe			Ball			2	efin	ed							fine	d Ul	
							sd u								ung	1/11-01	uad Co	re / VB	Process	sor Ba	llTnfo	rmatic				
					R								nde	ill.	Ū	/ U Q		<i>ic</i> / <i>i</i>	roces.	30, 20	defil	nee				
											ssor	Ball	Мар	(Lov	ver R	ight,	Colu	mns	23-1							
¢.	АА	23	22	21	20	19 	18 	17	16	15	14	13	12	11	10	9	8	7	6	5	4 VSS	3	2 VSS	1 VCCATS _1p8		
udei	Y W			VSS	VSS	VSS	M_1p0	VSS	VCCPGP PC	PD		VSS	SD DAT	GPP_G4	sd_cd	VSS	GPP_G6 J SD CLK	/	VSS		 GPP_C1 0 / UART0_	 GPP_C6 / SML1CL	Ī	GPP_C5	0 V	×1
	v			VCCPRI M_CORE	VCCPRI M_CORE	VCCPRI M_3p3	VSS	VSS	VSS	VCCAPL L_1P0			Ā2	Ā3	* 0						RTS#	K GPP_C7 / SML1DA TA	GPP_D2	ERT# GPP_D2 1/ SPI1_IC 2		
	U			iner	Jun							eDP_VD DEN	RSVD	RSVD	VSS	GPP_C1 97 I2C1_S CL	GPP_C1 87 I2C1_S DA	GPP_C1 67 12C0_S DA	GPP_C1 77 12C0_S CL		GPP_D1 67 ISH_UA RT0_CT S# / SML0BA LERT#	GPP_D1 57 ISH_UA RT0_RT	GPP_D1 4/ ISH_UA RT0_TX D7 SML0B0 LK / I2C4B	GPP_D1 3/ ISH_UA RT0_RX D/ SML0BC ATA / I2C4B_ SDA		
	т		<u>n</u> de	VSS	VCCSRA M_1P0	VCCSRA M_1P0	VSS	VSS	VCCPGP PE	VSS	95.				 GPP_C2	 GPP_C3	 GPP C1	 GPP_C0	e (i+1)		VSS		VSS	SDA VCCPRI M_1p0		
-9e	R P			VSS	VSS	VSS	 VCCPRI	VSS	VCCMPH	VCCMPH		VSS	eDP_BK LTEN	eDP_BK LTCTL	SMBALE RT#	/	SMBDAT A		VSS		 GPP_D1	 L GPP_D1	GPP DS	 GPP_D1 2	~	und
7110	N			VSS	VCCCLK	VSS	M_1P0 VCCAPL LEBB_1 P0	VCCMPH	VCCMPH VCCMPH YGT_1P 0	VCCMPH		VSS	GPP_E2	GPP_E2	vssy	GPP_E1 67 DDPE_H PD3	GPP_E2	GPP_E2	VSS		1 GPP_D5	0 GPP_De / ISH_I20 0_SCL	GPP_D8 / ISH_I20 1_SCL	GPP_D7	ev	
	м					Ge.				 VCCAM-		 GPP_E1	 GPP_E1	e	 GPP_E1	 GPP_E1		 GPP_E1	 GPP_E1		/ ISH_I20 0_SDA	SPI1 M	I SPI1_C	T		
	L			VCCCLK	VSS		VSS	VSS VCCMPH	VSS	PHYPLL _1P0	 24	8 / DDPB_C TRLCEK	97 DDPB_C TRLDAT A		GPP_E1 7 / EDP_HP D			47 DDPC_H PD1	57 DDPD_ HPD2	<u>6</u>	VSS		VSS	P0		
		VCCSA VCCSA	VSS VCCSA	VccPLL	VccPLL	2	VSS	VCCMPH YAON_1 P0	VSS	PHYPLL _1P0	<u>,</u>	VSS		VSS	USB3_3 _RXN		VSS	 10	USB3_2 _RXN / SSIC_R XN	GPP_D2 37 125 MC	GPP_D3	B GPP_E6	DEVSLF	GPP_E4		
und	н			VSSSA_ SENSE	VCCSA_ SENSE		VSS	uné	PCIE3_ RXN	VSS		PCIE1_ RXN / USB3_5 _RXN		RSVD	USB3_3 _RXP	nde	USB3_1 _RXN		XN USB3_2 _RXP / SSIC_R XP	LK GPP_D1 97 DMIC_C LK0	. OSI	2 GPP_E1 / SATAXF CIE1 / SATAGF 1	1 GPP_EC / SATAXF CIE0 /	0 GPP_E8 / SATALE		, ur
	G	VCCSA	VSS	PCIE8_ RXN / SATA1A _RXN PCIE8_	VCCSTG	nde	PCIE6_ RXN		PCIE3_ RXP	PCIE4_ RXN		PCIE1_ RXP / USB3_5 _RXP		PCIE2_ RXN / USB3_6 _RXN PCIE2_	VSS		USB3_1 _RXP		VSS	VSS	GPP_E2 / SATAXF CIE2 / SATAGF 2		CL_DAT A	CL_RST #		
	F	VSS	VSS	RXP / SATA1A _RXP	RXN / SATA0_ RXN PCIE7_ RXP /		PCIE6_ RXP		PCIE5_ RXN	PCIE4_ RXP		VSS	$\gamma_{\eta_{j}}$	RXP / USB3_6 _RXP			VSS		RSVD	PCIE_R COMPN	O.		VSS	VSS		
		PCIE9_ RXP PCIE10_ TXN	PCIE9_ RXN VSS	PCIE8_T XN / SATA1A	SATA0_ RXP PCIE6_T XN	PCIE5_T	VSS	PCIE3_T	PCIE5_ RXP PCIE2_T XN / USB3_6	VSS USB3_4 _TXP	VSS	USB3_1 TXP	RSVD	VSS	USB3_4 _RXN	 GPP_E1 17	ITP_PM ODE GPP_D1 77 DMIC_C	GPP_D2 07 DMIC_D	VSS	PCIE_R COMPP	RSVD	RSVD	RSVD	RSVD	_	
ini	(e	PCIE10_ TXP		PCIE8_T XP / SATA1A _TXP	XN PCIE6_T XP	XP PCIE5_T XN		XN PCIE3_T XP	_TXN PCIE2_T			USB3_1 _TXN	RSVD	RSVD		GPP_F1	GPP_D1 8/ DMIC_D ATA1	AIAU		VSS	RSVD		RSVD	VSS		d u
3	в	PCIE9_T XN	VSS	_TXP PCIE7_T XN / SATA0_ TXN		PCIE4_T XN	VSS	PCIE1_T XN / USB3_5 _TXN		USB3_3 _TXN	VSS	USB3_2 _TXN/ SSIC_T XN		RSVD	VSS	C1# GPP_E1 27 USB2_C C3#	ATA1	GPP_D4 / FLASHT RIG	SYS_PW ROK	/ SYS_RE SET#		RSVD	RSVD	nde		
	A P	PCIE9_T XP	VCCSTG			PCIE4_T XP	VCCST			USB3_3 _TXP				RSVD	VCCCLK				GPP_E3	VSS	RSVD	RSVD	8 <u>0</u>			
ed un	_	_	_	reti	neo		_	_	_	_	_	nin.	ed v		_	_	_	_	_	0	Jun	0.0	_	_		
			d un							2	und)e ₁₁ .							nde	tine						
	<i>9</i> e	Still.							def									ed /								ed V
20							Ain	ed u								d un							- 6	und	Stil.	
			132	2		und							~6'	JUUGe	fli.				Data	asheet,	, Volun	ne 1 of	2 2	undf		
			d V		1.						, ur	definition	16-							etine						
		SIL								ine	ġ.							6	uns							<u> </u>

Figure 9-6 11/11-0113 nc 22-11 Colur



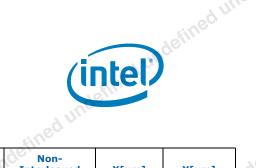
/YProcessor BallInformation U/U-Quad Core Processor Ball List (Sheet 1 of 39)

9-1. U/U- all Name 5 TXP / P TXP XP / XP / XP / XP / XA XN XN XN XN XN XN XN XN XN XN XN	Quad Core P	Processor Ba	Il List (Shee	t 1 of 39)	Non- Interleaved (NIL)	X[um] 14988.794 14313.154 13186.41 12510.77 11835.13 10708.386 10032.746 9357.106 8230.362 7554.722	-11314.1
TXP / P TXP XP / TXP XP / SATAO_TXP XP XP / SATAO_TXP XN XN XN XN XN XN XN			DDR4		Interleaved	14988.794 14313.154 13186.41 12510.77 11835.13 10708.386 10032.746 9357.106 8230.362	-10989.0 -11314.1 -11314.1 -10989.0 -11314.1 -11314.1 -10989.0 -11314.1
TXP / P TXP TXP XP / TXP XP XP / SATA0_TXP XP TXN / XN KP3 I10	under under underimed	undefined	undefined	undefined t	ndefined	14313.154 13186.41 12510.77 11835.13 10708.386 10032.746 9357.106 8230.362	-11314.1 -11314.1 -10989.0 -11314.1 -11314.1 -10989.0 -11314.1
P 	undetined	undefilmed	undefined	undefined	ndefined un	13186.41 12510.77 11835.13 10708.386 10032.746 9357.106 8230.362	-11314.1 -10989.0 -11314.1 -11314.1 -10989.0 -11314.1
P 	undefined	undefined	undefined	undefined	ndefined un	12510.77 11835.13 10708.386 10032.746 9357.106 8230.362	-10989.0 -11314.1 -11314.1 -10989.0 -11314.1
xp / xp / xp / xp / SATA0_TXP xp / SATA0_TXP xp xp xx / xx	undetined	undefined	undeined	undefined	ndefined un	11835.13 10708.386 10032.746 9357.106 8230.362	-11314.1 -11314.1 -10989.0 -11314.1
XP / TXP XP XP / SATA0_TXP XP TXN / XN KP3 I10	undefined	undefined	undefined	undefined	ndetined un	11835.13 10708.386 10032.746 9357.106 8230.362	-11314.1 -10989.0 -11314.1
TXP XP XP / SATA0_TXP XP TXN / XN KP3 110	undefined		undefined	undefined	ndefined	10032.746 9357.106 8230.362	-10989.0 -11314.1
XP XP / SATA0_TXP XP TXN / XN KP3 110	undefined		undefined	undefined	ndeti	10032.746 9357.106 8230.362	-10989.0 -11314.1 -11314.1
XP / SATA0_TXP XP TXN / XN KP3 I10	undefined		undefined	undefined	~~~~	9357.106 8230.362	-11314.1
XP / SATA0_TXP XP TXN / XN KP3 I10	under		undefined	undefinet		8230.362	
KP TXN / XN KP3 110			undefined	UNDE			
TXN / XN KP3 110			undefined				-10989.0
XN KP3 110			undefine			6879.082	-11314.1
KP3 110		6	Uno.	1		5752.338	-11314.1
10						5076.698	-10989.0
8		^O Dia			d'u	4401.058	-11314.1
		der			Ano	3274.314	-11314.1
		d ville			INGE	19348.958	-11314.1
	fine	~		eò		2598.674	-10989.0
16	, noe			Aetin-		1923.034	-11314.1
17	à Vi			a unu		796.29	-11314.1
16/11/			cine	D.		120.65	-10989.0
lo unos			der			-554.99	-11314.1
13			d un			-1681.734	-11314.1
		sine			ed	-2357.374	-10989.0
		nde.			1 efilte	18698.718	-11314.1
PCIE_P4		du.			uno	-3033.014	-11314.1
PCIE_P1	ining the second			e ^C		-4159.758	-11314.1
	unos			dern		-4835.398	-10989.0
I[2]	ed -			JUN		-5511.038	-11314.1
1[3]			06-	87			-11314.1
Junz			""der				-10989.0
			du.				-11314.1
ואנצן		1924			09 ₀₁₂		-11314.1
		, unor			odelin.		-11314.1
		ed -			d un-	-10467.086	
		r		200		10-07.000	-11 < 1/1 1
G_TDO	- Yetli					-11593.83	-11314.1
	PCIE_P4 PCIE_P1	3 PCIE_P4 PCIE_P1 [2] [3]	3	3	3	3	0 Image: Constraint of the system of the syste



B2. Table 9-1. U/U-Quad Core Processor Ball List (Sheet 2 of 39)

	(intel)			under			define	
ind	Table 9-1. U/U-0	Quad Core P	rocessor Ba) Ill List (She	et 2 of 39)	sined u		
Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- Interleaved (NIL)	X[um]	Y[um]
A59	JTAGX	der			enne		-12945.11	-11314.1
A6	GPP_E3 / CPU_GP0	. 0.1			Inos		17466.818	-10989.0
A61	PROC_TDO	~			0		-14071.854	-11314.1
A62	VCCGT			ACTIN			-14747.494	-10989.0
A63	VIDSCK			uno			-15423.134	-11314.1
A65	SKTOCC#			p.			-16549.878	-11314.1
A66	VCCGT		Yethi			Sinet	-17225.518	-10989.0
A67	VSS		, une			del	-17901.158	-11314.1
A68	PROCPWRGD	an ^e	0		6		-18551.652	-11314.1
A69	RSVD	detti			sine		-19201.892	-11314.1
A7	GPP_E7 / CPU_GP1	2 Une			nde		16791.178	-11314.1
A70	VSS	0.			0.		-19852.132	-11314.1
A9	GPP_E9 / USB2_OC0#			illo i			15664.434	-11314.1
AA1	VCCATS_1p8			inde			19989.038	-510.54
AA2	VSS			do V		2	19338.798	-510.54
AA4	VSS		16/10			cin ^{e0}	18363.438	-510.54
AA63	VCCGT		11000			-ge _{tti}	-15112.492	-595.63
AA64	VCCGT		2 0			<i>un</i> ^o	-15762.732	-595.63
AA65	VSS	76 ₁₁₁			ein ^e		-16412.972	-595.63
AA66	VCCGT	, unc			dell		-17063.212	-595.63
AA67	VCCGT	60			-dull'		-17713.452	-595.63
AA68	VSS			12			-18363.692	-595.63
AA69	VCCGT						-19013.932	-595.63
AA70	VCCGT			0			-19664.172	-595.63
AA71	VCCGT		ija.			e de la construcción de la const	-20314.412	-595.63
AB1	GPP_C8 / UART0_RXD		inde.			YG, II.	20314.158	152.4
AB10	USB2P_1		ed V			, unu	14984.476	-133.09
AB10 AB11	GPP_G0 / SD_CMD	194				0	14334.236	-133.09
AB11 AB12	GPP_G2 / SD_DATA1	Inou			dell'		13683.996	-133.09
AB12	GPP_G1 / SD_DATA0	ed			June		13033.756	-133.09
AB15 AB15	VSS	· ·		ć	neu		12188.19	-133.09
AB15 AB16	VSS			~de7			11537.95	-8.89
AB10 AB17	VCCPRIM_1p0			d'n.			10887.71	-8.89
AB17 AB18	VSS		Â.	n ^e		2	10237.47	-8.89
AB10	VCCPRIM_1P0			P		16111	9587.23	-8.89
AB19 AB2	GPP_C9 / UARTO_TXD		ned UN			, uno-	19663.918	152.4
AB20	VCCPRIM_1P0		no la companya de la comp			ed -	8936.99	-8.89
		- inde			ACtil		8936.99	-8.89
ADZI	••••	ined u.			ed und		8280.75	-0:05
	d unde			Inde	fill.	Detector	Jefi	neu
	134			stined unde		Datasneet	:, Volume 1 of 2	<u><</u>
	June		+ unde			ndefin		



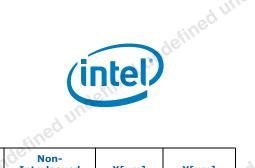
/YProcessor BallInformation U/U-Quad Core Processor Ball List (Sheet 3 of 39)

AB3 GPP_C11 / UART0_CTS# Image: Ctrain of the second seco		U/U-Quad Core/YProces	ssor BallInform	ation	ndefine		Ľ	ntel	1
Ball # Ball Name DDR1 LPDDR3 DDR4 Interleaved (IL) Interleaved (IL) X[um] Y[u AB3 GPP_C11 / UARTO_CT5# 19013.678 155 AB4 GP_SI / UARTO_CT5# 19013.678 155 AB4 GP_SI / UART_CT5# 17385.436 133 AB5 CCOPC 16384.356 133 AB5 SD_BCOMP 16384.356 133 AB6 USEX_1 16384.356 133 AB6 USEX_1 16384.356 133 AB7 SD_BCOMP 19989.08 815 AC8 VSS 19989.08 815 AC8 VCCOT 19338.78 815 AC64 VCCGT 19163.322 318 <tr< th=""><th>nde</th><th>Table 9-1. U/U-0</th><th>Quad Core P</th><th>rocessor Bal</th><th>″ Il List (Shee</th><th>et 3 of 39)</th><th>sined uns</th><th></th><th></th></tr<>	nde	Table 9-1. U/U-0	Quad Core P	rocessor Bal	″ Il List (Shee	et 3 of 39)	sined uns		
Abs GPP_C15/LMATL_CTS# 1833.438 155 ABS USS2_COMP 17585.436 133 ABS USS2_COMP 16935.196 133 ABS VSS 16935.196 133 ABS USS2 16935.196 133 ABS USS2 16935.196 133 ABS USS2 15634.716 133 ABS USS2 19989.038 815 AC1 SF_UARTL_RD/ 19989.038 815 AC2 SF_UARTL_RD/ 19338.798 815 AC3 VCCPC_SENSE 16688.558 815 AC4 VCCGT 15112.492 318 AC55 VCCGT 16412.972 188 AC66 VCCGT 17065.212 318 AC66 VCCGT 14913.932 318 AC66 VCCGT 1903.932 318 AC70 VCCGT 1903.932 318 AC71 VCCGT 19043.412 318	Ball #	Ball Name	DDR3L	LPDDR3	DDR4		Interleaved	X[um]	Y[um
Abs / ISH_LIARTL_CTS* I and interpreter I and interpret I and inter I and interpret	AB3	GPP_C11 / UART0_CTS#	udell			16/11/6		19013.678	152.4
AB6 USB2_COMP 1758,436 -133 AB7 SD_RCOMP 16935.196 -133 AB7 SD_RCOMP 16935.196 -133 AB8 VSS 11524.4766 -133 AB9 USB2N_1 15534.716 -133 AB1 SD_RCOMP 19980.038 815 CC GPP_C12/UARTL_RXD/ 19338.798 815 AC2 GFP_C13/UARTL_RXP 19338.798 815 AC3 YCCPC_SENSE 19338.798 815 AC64 VCCGT 19338.798 815 AC65 VCCGT 15124.992 318 AC66 VCCGT 1763.212 318 AC66 VCCGT 17063.212 318 AC66 VCCGT 1793.392 318 AC70 VCCGT 1933.798 8147 AC71 VCCGT 1901.392.318 314 AC70 VCCGT 1901.392.318 314 AC70 VCCGT 1901.392.318 3	AB4	GPP_C15 / UART1_CTS#	0.			JULO		18363.438	152.4
AB62 VCCOPC Image: second sec		<u> </u>			09/10			17585.436	-133.09
AB7 SD_RCOMP Image: solution of the s	-				dein				-138.4
A88 VSS 112249.56 -133 A89 USB2N.1 15634.716 -133 AC1 GPP_C12/UART_RXD/ ISM_UART_RXD/ ISM_UART_RXD/ AC2 19989.038 815 AC2 GPP_C13/UART_RXD/ ISM_UART_RXD/ ISM_UART_RXD/ ISM_UART_RXS 19338.798 815 AC3 GPP_C14/UART_RTS 19338.798 815 AC63 VCCOC 19338.798 815 AC64 VCCGT 18688.558 815 AC65 VCCGT 11562.732 318 AC66 VCCGT 11563.212 318 AC66 VCCGT 117713.452 318 AC67 VCCGT 11998.32.23 318 AC68 VCCGT 11998.32.23 318 AC69 VCCGT 11998.32.23 318 AC69 VCCGT 11998.32.23 318 AC70 VCCGT 11998.32.23 318 AC11 VCCGT 11998.42.23 318 AD11 GPP_C20/UART_RXD 12031.412 318				à	une		n		-133.09
AB9 USB2N_1 Image: CPP_C12 / UART1_RXD / SP_C12 / SP_C12 / UART1_RXD / SP_C12 / SP_C12 / SP_C12 / UART1_RXD / SP_C12		812.		sines					-133.09
ACIISH_LARTL_RXDISH_LARTL_RXDISH_LARTL_RXDISH_LARTL_RXDAC2GPP_CL1/URTL_RTS/FISH_LARTL_RXDISH_LARTL_RXDISH_LARTL_RXDAC3GPP_CL1/URTL_RTS/FISH_LARTL_RXDISH_LARTL_RXDAC4VCCGTISH_LARTL_RXDISH_LARTL_RXDAC64VCCGTISH_LARTL_RXDISH_LARTL_RXDAC65VCCGTISH_LARTL_RXDISH_LARTL_RXDAC66VCCGTISH_LARTL_RXDISH_LARTL_RXDAC67VCCGTISH_LARTL_RXDISH_LARTL_RXDAC68VCCGTISH_LARTL_RXDISH_LARTL_RXDAC69VCCGTISH_LARTL_RXDISH_LARTL_RXDAC70VCCGTISH_LARTL_RXDISH_LARTL_RXDAC71VCCGTISH_LARTL_RXDISH_LARTL_RXDAC71VCCGTISH_LARTL_RXDISH_LARTL_RXDAC71VCCGTISH_LARTL_RXDISH_LARTL_RXDAD10GPP_C20 / UARTL_RXDISH_LARTL_RXDISH_LARTL_RXDAD11GPP_C20 / UARTL_RXDISH_LARTL_RXDISH_LARTL_RXDAD13VSSISH_LARTL_RXDISH_LARTL_RXDAD14GPP_C11/URTL_RXDISH_LARTL_RXDISH_LARTL_RXDAD15VCCSW_J3AISH_LARTL_RXDISH_LARTL_RXDAD16GPP_C11/URTL_RXDISH_LARTL_RXDISH_LARTL_RXDAD17GPP_C11/URTL_RXDISH_LARTL_RXDISH_LARTL_RXDAD18VCCSW_J3AISH_LARTL_RXDISH_LARTL_RXDAD19VSSISH_LARTL_RXDISH_LARTL_RXDAD19VSSISH_LARTL_RXDISH_		USB2N_1		nder			1.etine		-133.09
AC ISH_UART1_TXD ISH_UART1_RTSA AG3 GPC_14/UART1_RTSA ISH_UART1_RTSA ISH_UART1	AC1	GPP_C12 / UART1_RXD / ISH_UART1_RXD	sined	$\mathcal{O}_{\mathcal{F}}$		ed l	no	19989.038	815.34
ACG /TSH_UARTI_RTS# Image: Constraint of the second o	AC2	ISH_UART1_TXD	under			define		19338.798	815.3
AC64VCCGTImage: sector s		/ ISH_UART1_RTS#			ed	UI.			815.34
ACCSVCCGTImage: selection of the selecti					defin				318.7
Acces VCCGT Image: Constraint of the constrai					une				318.7
AccorVCCGTImage: Accord and a stress of the stress o		e'''		erne'	P		d V		318.7
Acces VCCGT Image: Constraint of the constrai				der.			in since		318.7
Action VCCGT Interview <	6			, U'			uno~		318.7
AC70VCCGTImage: selection of the selecti						ed	0.		318.7
AC71VCCGTImage: Constraint of the constraint of th			<u>nde</u> .			Yelli,			6.5
AD1GPP_C20 / UART2_RXDImage: Constraint of the con			70.			1 UNC.			
AD10 USB2P_4 Image: constraint of the second s		. 1/3			9773	0			
AD11GPP_F10 / 12C5_SDA / ISH_12C2_SDAIIIIAD12GPP_F11 / 12C5_SCL / ISH_12C2_SCLIII </td <td></td> <td></td> <td></td> <td></td> <td>,dell'</td> <td></td> <td></td> <td></td> <td></td>					,dell'				
AD13VSSImage: selection of the selection		GPP_F10 / I2C5_SDA /		sine	d un		ad V	00-	933.70
AD15 VCCPGPPG Image: Constraint of the co	AD12	GPP_F11/ I2C5_SCL / ISH_I2C2_SCL		unden			define	13683.996	933.70
AD16VSSImage: selection of the selection	AD13	VSS		0		6	UL	13033.756	933.70
AD17 VCCDSW_3p3 Image: constraint of the second secon	AD15	VCCPGPPG	defini			sine		12188.19	829.3
AD18 VCCDSW_3p3 Image: constraint of the second secon	-		, un			der		11537.95	829.3
AD19 VSS Image: Marcine Marci	AD17		2 ¹			d		10887.71	829.3
AD2 GPP_C21 / UART2_TXD Image: Constraint of the constraint of	AD18				nije,				829.3
AD20 VSS Image: Constraint of the state of the s	AD19				nde				829.3
AD21 VSS Image: Constraint of the state of the s					ed r				1478.2
AD3 GPP_C22 / UART2_RTS# 19013.678 1478 AD4 GPP_C23 / UART2_CTS# 18363.438 1478 AD6 USB2N_2 17585.436 933.		<u>, , , , , , , , , , , , , , , , , , , </u>		Lefil 1	5		^{cineo}		829.3
AD4 GPP_C23 / UART2_CTS# 18363.438 1478 AD6 USB2N_2 17585.436 933.				unu			dell		829.3
AD6 USB2N_2 17585.436 933.				eo			λu_{I}		1478.2
			Jein,			9nine			1478.2
AD62 VSS -14643.862 775 Datasheet, Volume 1 of 2 135			un			nde.			933.70
ndefiner a undefiner		undefi	6-		hed undefil	ned .	-6	in ^e	775.9
	, ed l	unoz		d under			ndefine		



ed undefined undefined Table 9-1. U/U-Quad Core Processor Ball List (Sheet 4 of 39)

	Table 9-1. U/U-0	Quad Core P	rocessor Ba	ll List (She	et 4 of 39)	aned ut		
Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- Interleaved (NIL)	X[um]	Y[um]
AD7	USB2P_2	uder".			1.efine		16935.196	933.704
AD8	VSS	1 UN			Inob		16284.956	933.704
AD9	USB2N_4	r			20		15634.716	933.704
AE62	VCCEOPIO			16/11			-14643.862	1690.37
AE63	VSSOPC_SENSE			uno			-15112.492	1233.17
AE64	VSS		in ne	, C			-15762.732	1233.17
AE65	VSS		Aet.			sinet	-16412.972	1233.17
AE66	VSS		1 UNC			ndel	-17063.212	1233.17
AE67	VSS	an ^e	0		6	0.	-17713.452	1233.17
AE68	VSS	gerr.			fine		-18363.692	1233.17
AE69	VSS	2 UN			inde		-19013.932	1233.17
AF1	VSS	<u>.</u>			0		19989.038	2141.22
AF10	VSS			ille i			14984.476	2000.50
AF11	GPP_F8 / I2C4_SDA			Ince			14334.236	2000.50
AF12	GPP_F9 / I2C4_SCL			6 <u>0</u>		2	13683.996	2000.50
AF13	GPP_F23		ACTIN			cinet.	13033.756	2000.50
AF15	VSS		, uno			der	12188.19	1667.51
AF16	VCCPGPPF		20			1 vili	11537.95	1667.51
AF17	VSS	deth			Sine		10887.71	1667.51
AF18	VCCPRIM_CORE	1 Une			nder		10237.47	1667.51
AF19	VCCPRIM_CORE	e ^o			d'		9587.23	1667.51
AF2	VSS			2	10		19338.798	2141.22
AF20	VCCSRAM_1P0			inde.			8936.99	1667.51
AF21	VCCSRAM_1P0			00			8286.75	1667.51
AF4	VSS		1erii			cin ^{ec}	18363.438	2141.22
AF6	USB2N_6		inoc			-96th	17585.436	2000.50
AF63	VSS		ed			2 UNG	-15112.492	2147.57
AF64	DDR1_DQ[1] / DDR0_DQ[17]	Indefi			DDR1_DQ[1]	DDR0_DQ[17]	-15762.732	2147.57
AF65	DDR1_DQ[0] / DDR0_DQ[16]	nedt			DDR1_DQ[0]	DDR0_DQ[16]	-16412.972	2147.57
AF66	DDR1_DQ[4] / DDR0_DQ[20]			. 40	DDR1_DQ[4]	DDR0_DQ[20]	-17063.212	2147.57
AF67	DDR1_DQ[5] / DDR0_DQ[21]			ed un	DDR1_DQ[5]	DDR0_DQ[21]	-17713.452	2147.57
AF68	DDR1_DQ[9] / DDR0_DQ[25]		de		DDR1_DQ[9]	DDR0_DQ[25]	-18363.692	1939.03
AF69	DDR1_DQ[13] / DDR0_DQ[29]		red un		DDR1_DQ[13]	DDR0_DQ[29]	-19013.932	1939.03
AF7	USB2P_6	10	<i>.</i>		213	e	16935.196	2000.50
AF70	DDR1_DQ[8] / DDR0_DQ[24]	dunc			DDR1_DQ[8]	DDR0_DQ[24]	-19664.172	1839.97
	136	IUL		fined und	atineo	Datasheet	, Volume 1 of 2	led un.



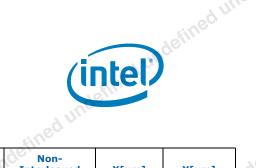
/YProcessor BallInformation U/U-Quad Core Processor Ball List (Sheet 5 of 39)

de			red	Inden		intel			
Ball #	Table 9-1. U/U-(Ball Name	Quad Core P	LPDDR3	II List (Shee DDR4	Interleaved (IL)	Non- Interleaved (NIL)	X[um]	Y[um	
AF71	DDR1_DQ[12] / DDR0_DQ[28]	Indetti			DDR1_DQ[12]	DDR0_DQ[28]	-20314.412	1839.9	
	USB2N_8			2	UNC.		16284.956	2000.5	
AF9	USB2P_8			cine			15634.716	2000.5	
AG1	USB2N_9			dell			20314.158	2804.3	
AG15	VCCPGPPB		6-	Ú.		771	12188.19	2505.	
AG16	VSS		sines			60	11537.95	2505.	
AG17	VSS		nde.			16/11/1	10887.71	2505.	
AG18	VSS	6				100- 100-	10237.47	2505.	
AG19	VSS	Alle			ined.		9587.23	2505.	
AG2	USB2P_9	Inde			dein		19663.918	2804.	
AG20	VSS			د	Un		8936.99	2505.3	
AG21	VSS			eine	1		8286.75	2505.	
AG3	USB2_ID			ger.			19013.678	2804.	
AG4	USB2_VBUSSENSE		2	UN			18363.438	2804.	
AG62	VCCEOPIO		ine'	e*		ed u	-14643.862	2604.	
AG69	DDR1_DQSN[1] / DDR0_DQSN[3]		under		DDR1_DQSN[1]	DDR0_DQSN[3]	-18688.812	2601.9	
AG70	DDR1_DQSP[1] / DDR0_DQSP[3]	etine	<u>A</u>		DDR1_DQSP[1]	DDR0_DQSP[3]	-19339.052	2502.9	
AG71	VSS	INOS			dern		-19989.292	2502.9	
AH1	USB2N_7	9			A UM		19989.038	3467	
AH10	GPP_F5 / I2C2_SCL			e in P			14984.476	3067.3	
AH11	GPP_F6 / I2C3_SDA			der			14334.236	3067.3	
AH12	GPP_F7 / I2C3_SCL			y un			13683.996	3067.3	
AH13	VSS		sine			ed t	13033.756	3067.3	
AH2	USB2P_7		der			ofine	19338.798	3467	
AH3	USB2N_3		6 01			inos	18688.558	3467	
AH6	VSS	-fine	2		e C		17585.436	3067.3	
AH63	VSS	nde			76th		-15112.492	3061.	
AH64	VSS	,0			, une		-15762.732	3061.	
AII05	DDR1_DQSP[0] / DDR0_DQSP[2]			nine (DDR1_DQSP[0]	DDR0_DQSP[2]	-16412.972	3061.	
Anoo	DDR1_DQSN[0] / DDR0_DQSN[2]			d unoc	DDR1_DQSN[0]	DDR0_DQSN[2]	-17063.212	3061.	
	VSS		212	67		6	-17713.452	3061.	
AI100	DDR1_DQ[11] / DDR0_DQ[27]		unde.		DDR1_DQ[11]	DDR0_DQ[27]	-18363.692	3165.8	
AII05	DDR1_DQ[15] / DDR0_DQ[31]	Nija .	ev		DDR1_DQ[15]	DDR0_DQ[31]	-19013.932	3165.8	
	USB2N_10	nde.			Jefin'		16935.196	3067.3	
AH70	DDR1_DQ[14] / DDR0_DQ[30]	ed u	ned undefi		DDR1_DQ[14]	DDR0_DQ[30]	-19664.172	3165.8	



B2. Table 9-1. U/U-Quad Core Processor Ball List (Sheet 6 of 39)

	(intel)			1efine	U/U-Quad Co	ore/YProcessor Ba	allInformation	1
	d UIT			uno			9611	
	efine					d un		
nu	Table 9-1. U/U-0	Quad Core P	rocessor Ba	all List (She	et 6 of 39)	siner		I
Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- Interleaved (NIL)	X[um]	Y[um]
AH71	DDR1_DQ[10] / DDR0_DQ[26]	Inder			DDR1_DQ[10]	DDR0_DQ[26]	-20314.412	3165.856
AH8	USB2P_10				1 UNC		16284.956	3067.304
AH9	GPP_F4 / I2C2_SDA			1012			15634.716	3067.304
AJ1	USB2N_5			der			20314.158	4130.04
AJ15	VSS			1 vil.			12188.19	3343.91
AJ16	VCCSPI		nia.			60	11537.95	3343.91
AJ17	VCCDSW_3p3		nder.			1etine	10887.71	3343.91
AJ18	VSS		<u>d</u>			uno	10237.47	3343.91
AJ19	VCCHDA	FILE			ed		9587.23	3343.91
AJ2	USB2P_5	nde			76111		19663.918	4130.04
AJ20	VSS	0			, une	1	8936.99	3343.91
AJ21	VCCPRIM_3p3	r			(⁰	+	8286.75	3343.91
AJ3	USB2P_3			Ye.			19013.678	4130.04
AJ4	VSS			1 000			18363.438	4130.04
AJ62	VSSEOPIO_SENSE		225	, 0 0		6	-14643.862	3519.17
AK10	GPP_F3 / I2S2_RXD		-gelli.			fines	14984.476	4007.104
AK11	VSS		7.00			nde.	14334.236	4007.104
AK11	RSVD_TP	7773	20		0	6. V.	13683.996	4007.104
AK12	RSVD_TP	deit			i ciino		13033.756	4007.104
AK15 AK15	VCCPGPPA	- d Ul.			inde		12188.19	4182.11
AK15 AK16	VSS	00			ed		11537.95	4182.11
AK10 AK17	VCCRTCPRIM_3p3			i i	10-		10887.71	4182.11
AK17 AK18	VSS			10°			10237.47	4182.11
	VCCRTC			ed -				
AK19	VCCPRIM_1p0		7681			99773	9587.23	4182.11
AK20			, unu			dell'	8936.99	4182.11
AK21	VSS		e ⁰			∂u_{II}	8286.75	4182.11
AK22	VSS VCCSA	dett				87	7595.616	4009.136
AK23	VCCSA	June			uger.		6681.216	4009.130
AK25		ne ^U			d'UN		5766.816	4009.136
AK27	VSS				in ^c		4852.416	4009.136
AK28	VCCIO			, nde			3938.016	4009.136
AK30	VCCIO			ed v.			3023.616	4009.136
AK32	RSVD		10	10-		eine	2109.216	4009.136
AK33	VCC		, unde			defin	1194.816	4009.136
AK35	VCC		Loo T			Jun	280.416	4009.136
AK37	VCC	10			255	e	-633.984	4009.136
AK38	VCC	, unos			dein		-1548.384	4009.136
AK40	VCC	ned -			d Ulli		-2462.784	4009.136
	138 undefined undef			stined und				ed v
	A UNS			.ndi			Jefil	~~~
	138			du.		Datasheet	, Volume 1 of 2	2
	der		. 6	sinc				
	UI.		nde			ACTIV		
			du.			, inc.		



/YProcessor BallInformation U/U-Quad Core Processor Ball List (Sheet 7 of 39)

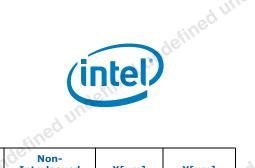
	U/U-Quad Core/YProce	SSOF BAILINTORM	acion	intel					
nde	Table 9-1. U/U-	Quad Core P	rocessor Ba	Ill List (Shee	et 7 of 39)	sined une			
Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- Interleaved (NIL)	X[um]	Y[um]	
AK42	VccGTx	dell			1efine		-3377.184	4009.13	
AK43	VccGTx	0.1			unos		-4291.584	4009.13	
AK45	VccGTx			e Ó			-5205.984	4009.13	
AK46	VccGTx			Actin			-6120.384	4009.13	
AK48	VccGTx			una		~	-7034.784	4009.13	
AK50	VccGTx		cine ^o			duit	-7949.184	4009.13	
AK52	VccGTx		dethi			since	-8863.584	4009.13	
AK53	VccGTx	2	Une			nde.	-9777.984	4009.13	
AK55	VccGTx	cine ^o			6		-10692.384	4009.13	
AK56	VccGTx	deit			sine		-11606.784	4009.13	
AK58	VccGTx	V		1	Inde		-12521.184	4009.13	
AK6	GPP_F0 / I2S2_SCLK				0		17585.436	4007.10	
AK60	VccGTx			1efine	1		-13435.584	4009.13	
AK62	VCCGTx_SENSE			Jnor	1		-14459.712	4143.75	
AK63	VSS			<u> </u>			-15112.492	3976.3	
AK64	DDR1_DQ[3] / DDR0_DQ[19]		indefilie		DDR1_DQ[3]	DDR0_DQ[19]	-15762.732	3976.3	
AK65	DDR1_DQ[2] / DDR0_DQ[18]	tine			DDR1_DQ[2]	DDR0_DQ[18]	-16412.972	3976.3	
AK66	DDR1_DQ[7] / DDR0_DQ[23]	under			DDR1_DQ[7]	DDR0_DQ[23]	-17063.212	3976.3	
AK67	DDR1_DQ[6] / DDR0_DQ[22]	D.			DDR1_DQ[6]	DDR0_DQ[22]	-17713.452	3976.3	
AK68	VSS			fills			-18363.692	3828.79	
AK69	VSS			noe			-19339.052	3828.79	
AK7	GPP_F1 / I2S2_SFRM		. (,0,			16935.196	4007.10	
AK70	VccGTx		efini			tineo.	-19989.292	3828.79	
AK8	VSS		inde			derin	16284.956	4007.10	
AK9	GPP_F2 / I2S2_TXD		<u>,</u> ,		2	UNC	15634.716	4007.10	
AL1	DCPDSW_1p0	16th			sine		19989.038	4792.9	
AL2	VSS	, uno-			dei.		19338.798	4792.9	
AL23	VCCPLL_OC	8 0 -			dun		7138.416	4473.95	
AL25	RSVD			213	9 7		6224.016	4473.9	
AL27	RSVD			de''			5309.616	4473.95	
AL28	VSS			d V.			4395.216	4473.95	
AL30	VCCIO		113	(°-		ed	3480.816	4473.95	
AL32	VSS		.nde.			76111-	2566.416	4473.95	
AL33	VCC		0 V.		1	uno	1652.016	4473.95	
AL35	VSS	îi)o,				P -	737.616	4473.95	
AL37	VCC	. Inde			Y6,11,		-176.784	4473.95	
	VSS	ed V			1 Une			4473.95	
AL38	VSS Datasheet, Volume 1 of 2		189	ned undefi	ned U.	undefined	-1091.184	ja u	
tined			ed unc			d under.			

(intel) red undefine

U/U-Quad Core/YProcessor BallInformation

B2. Table 9-1. U/U-Quad Core Processor Ball List (Sheet 8 of 39)

	(intel)			retine	u/u-Quaa Co	re/YProcessor Ba	antniormation	I
				unu			der	
	etine		siner			d ul		
<u>nu</u>	Table 9-1. U/U-C	luad Core P	Processor Ba	nii List (She	et 8 of 39)	since		
Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- Interleaved (NIL)	X[um]	Y[um]
AL4	VSS	nde			164100		18363.438	4792.98
AL40	VCC) ().			uno		-2005.584	4473.95
AL42	VCCIO			1	0		-2919.984	4473.95
AL43	VccGTx			Yeu			-3834.384	4473.95
AL45	VSS			Un			-4748.784	4473.95
AL46	VccGTx		an ^e	p.		- d ¹	-5663.184	4473.95
AL48	VSS		der			fine	-6577.584	4473.95
AL50	VccGTx		y Un			nde	-7491.984	4473.95
AL52	VSS	ei n ^e	~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~		d		-8406.384	4473.95
AL53	VccGTx	dei			atine		-9320.784	4473.95
AL55	VSS	9 u.			INOS		-10235.184	4473.95
AL56	VccGTx				do v		-11149.584	4473.95
AL58	VSS			18fir			-12063.984	4473.95
AL60	VccGTx			. uno-			-12978.384	4473.95
AL61	VSSGTx_SENSE			eç .		2	-13892.784	4473.95
AL63	VCCEOPIO_SENSE		Actin			ein ^{eu}	-15112.492	4845.05
AL64	VSS		, uno-			der	-15762.732	4845.05
AL65	VSS		20			1 VIII	-16412.972	4845.05
AL66	VSS	Jeil.			Aine		-17063.212	4845.05
AL68	DDR0_DQ[1]	4 Une			nder		-18363.692	4491.73
AL69	DDR0_DQ[5]	60			od this		-19013.932	4491.73
AL70	DDR0_DQ[4]			ile.	0		-19664.172	4491.73
AL71	DDR0_DQ[0]			inde			-20314.412	4491.73
AM1	GPP_F20 / EMMC_DATA7			ed		2	20314.158	5455.92
AM10	GPP_B11 / EXT_PWR_GATE#		ndeti			lefinec	14910.816	4946.39
AM11	GPP_B2 / VRALERT#		du			uno	13996.416	4946.39
AM13	VSS	il)	Ne.			,o	13082.016	4946.39
AM15	GPD2 / LAN_WAKE#	noe			4em		12167.616	4946.39
AM16	RTCRST#	ed			1 UNC		11253.216	4946.39
AM18	RTCX1			ć	nec		10338.816	4946.39
AM2	GPP_F21 / EMMC_RCLK			de			19663.918	5455.92
AM20	RTCX2			dun			9424.416	4946.39
AM21	VSS		ć	ner		0	8510.016	4946.39
AM22	VSSIO_SENSE		nde			etine	7595.616	4946.39
AM23	VCCIO_SENSE		dun			Inoc	6681.216	4946.39
AM25	VSS	2	Ine			ed	5766.816	4946.39
AM27	VSS	nde			7641		4852.416	4946.39
AM28	VCCIO	du			, uno-		3938.016	4946.39
	101	Inc			cine ⁰			d un
	140 ad unoc			Inde		Datasheet	, Volume 1 of 2	
	140 undefined undef			fined unde		Datasheet	20	-
	Jun		nde			Lefin		
			du			unc		



/YProcessor BallInformation U/U-Quad Core Processor Ball List (Sheet 9 of 39)

	tined unor	ssor BallInform	ed l	Indefin		intel			
Ball #	Table 9-1. U/U-(Ball Name	Quad Core P	LPDDR3	II List (Shee DDR4	Interleaved (IL)	Non- Interleaved (NIL)	X[um]	Y[un	
AM3	GPP_F22 / EMMC_CLK	ndein			efines		19013.678	5455.	
AM30	VCCIO	0.1			inor		3023.616	4946.3	
AM32	VCC			. red			2109.216	4946.3	
AM33	VCC			Jerin .			1194.816	4946.3	
AM35	VCC			unu			280.416	4946.3	
AM37	VCC		ineo			dui	-633.984	4946.3	
AM38	VCC		detti			sinet	-1548.384	4946.3	
AM4	GPP_F19 / EMMC_DATA6	2	UN			nde.	18363.438	5455.	
AM40	VDDQC	sines			d'		-2462.784	4946.3	
AM42	VCCIO	den			efine		-3377.184	4946.3	
AM43	VSS	U.			Inde		-4291.584	4946.3	
AM45	VSS			-00	3		-5205.984	4946.3	
AM46	VSS			10fin			-6120.384	4946.3	
AM48	VccGTx			unos			-7034.784	4946.3	
AM5	GPP_B19 / GSPI1_CS#		e	<u>, </u>		A UT	17654.016	4946.	
AM50	VccGTx		A CTIT			sineu	-7949.184	4946.	
AM52	VccGTx	4	uno			dell	-8863.584	4946.	
AM53	VccGTx	00			6-	<u>)))</u>	-9777.984	4946.	
AM55	VSS	det			finee		-10692.384	4946.	
AM56	VccGTx	J UNC			nder		-11606.784	4946.	
AM58	VccGTx			0	0.00		-12521.184	4946.	
AM60	VSS			fine			-13435.584	4946.	
AM61	VSS			nde			-14349.984	4946.	
AM68	VSS		~?	Ò.		2 1	-18038.572	5055.	
AM69	DDR0_DQSP[0]		1 Stine			cin ^{eo}	-18688.812	5055.	
AM7	GPP_B23 / SML1ALERT# / PCHHOT#		d unoc			undein	16739.616	4946.	
AM70	DDR0_DQSN[0]	fin	7		eC		-19339.052	5154.	
AM71	VSS	noc			Actin		-19989.292	5154.	
AM8	VSS	20			4 UN		15825.216	4946.	
AN1	GPP_F17 / EMMC_DATA4			0.5	(CC		19989.038	6118	
AN10	GPP_B13 / PLTRST#			dem			14910.816	5596.	
AN11	GPP_B0 / CORE_VID0			dun			13996.416	5596.	
AN13	GPP_B1 / CORE_VID1		nia	80		6	13082.016	5596.	
AN15	SLP_SUS#		der			efine	12167.616	5596.	
AN16	GPD6 / SLP_A#		dui			INOC	11253.216	5596.	
AN18	SRTCRST#	li)_	0		~?	ð. T	10338.816	5596.	
AN2	GPP_F18 / EMMC_DATA5	.nde			76/11/2		19338.798	6118	
AN20	VSS	du		ned undefi	innos		9424.416	5596.	



ed undefined undefined Table 9-1. U/U-Quad Core Processor Ball List (Sheet 10 of 39)

	(intel)			stines	U/U-Quad Co	re/YProcessor Ba	llInformation	ī
	100			nde			retill	
	AINE							
nr.	Table 9-1. U/U-0	Quad Core P	Processor Ba	ll List (Shee	t 10 of 39)			
Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- Interleaved (NIL)	X[um]	Y[um]
AN21	DDR1_DQ[63]	dell			erine		8510.016	5596.636
AN22	DDR1_DQ[60]				INO		7595.616	5596.636
AN23	VSS						6681.216	5596.636
AN25	DDR1_DQ[54]			16111			5766.816	5596.636
AN27	DDR1_DQ[53]			una			4852.416	5596.636
AN28	VSS			<u>P</u>		20	3938.016	5596.636
AN3	GPP_F16 / EMMC_DATA3		Yeilli			sin ^{eu.}	18688.558	6118.86
AN30	VSS		, une			JOS !!	3023.616	5596.636
AN32	VSS	in ^e	2		6-	0.1	2109.216	5596.636
AN33	VSS	-yern.			-sines		1194.816	5596.636
AN35	VSS	2 UN			nde'		280.416	5596.636
AN37	VSS				Ó		-633.984	5596.636
AN38	VSS			iniz.	7		-1548.384	5596.636
AN40	VSS			inde			-2462.784	5596.636
AN42	VSS			20 U.			-3377.184	5596.636
AN43	DDR1_ALERT#		nife,			ineo.	-4291.584	5596.636
AN45	DDR1_CKN[0]		inde			detill	-5205.984	5596.636
AN46	DDR1_CKN[1]		60.0			un ^c	-6120.384	5596.636
AN40 AN48	DDR1_MA[11] / DDR1_CAA[7] /	DDR1_MA[11]	DDR1_CAA[7]	DDR1_MA[11]	define	0	-7034.784	5596.636
AN5	DDR1_MA[11] GPP_B22 / GSPI1_MOSI	60			June		17654.016	5596.636
ANJ	DDR1_MA[12] /	DDR1_MA[12]	DDR1_CAA[6]	DDR1_MA[12]	67		17034.010	5590.050
AN50	DDR1_CAA[6] / DDR1_CAA[6] / DDR1_MA[12]		DDKI_CAA[0]	unde			-7949.184	5596.636
AN52	DDR1_MA[14] / DDR1_CAA[9]/ DDR1_BG[1]	DDR1_MA[14]	DDR1_CAA[9]	DDR1_BG[1]		stined	-8863.584	5596.636
AN53	DDR1_MA[15] / DDR1_CAA[8]/ DDR1_ACT#	DDR1_MA[15]	DDR1_CAA[8]	DDR1_ACT#		d unde	-9777.984	5596.636
AN55	DDR1_CKE[2]	der			- fin		-10692.384	5596.636
AN56	DDR1_CKE[0]	dur			inde.		-11606.784	5596.636
AN58	VSS	Ver			ed t		-12521.184	5596.636
AN60	DDR1_DQ[27] / DDR0_DQ[59]			ndefi	DDR1_DQ[27]	DDR0_DQ[59]	-13435.584	5596.636
AN61	DDR1_DQ[28] / DDR0_DQ[60]			ed u.	DDR1_DQ[28]	DDR0_DQ[60]	-14349.984	5596.636
AN63	VSS		10			sine	-15264.384	5596.636
AN65	DDR1_DQ[19] / DDR0_DQ[51]		d unc		DDR1_DQ[19]	DDR0_DQ[51]	-16178.784	5596.636
AN66	DDR1_DQ[20] / DDR0_DQ[52]	_de	We-		DDR1_DQ[20]	DDR0_DQ[52]	-17093.184	5596.636
AN68	DDR0_DQ[2]	4 un			nde.		-18363.692	5718.556
	142	ine		tined unde	ined t		, Volume 1 of 2	led unc
e	June		4 unde			undefine		
AITT			cineu			du		

led underme U/U-Quad Core/YProcessor BallInformation



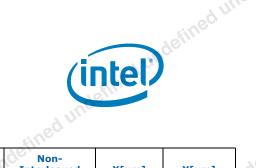
Jed undefined undefined U/U-Quad Core Processor Ball List (Sheet 11 of 39) Table 9-1.

AN69	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- Interleaved (NIL)	X[um]	Y[um]
7	DDR0_DQ[3]	nde			16911		-19013.932	5718.556
AN7	GPP_B20 / GSPI1_CLK	U. 1			une		16739.616	5596.636
AN70	DDR0_DQ[6]			ine ^o			-19664.172	5817.616
AN71	DDR0_DQ[7]			den			-20314.412	5817.616
AN8	GPP_B15 / GSPI0_CS#		2	une			15825.216	5596.636
AP1	GPP_F14 / EMMC_DATA1		sineu			du.	20314.158	6781.8
AP10	VSS		der			sine	14910.816	6246.876
AP11	GPP_A15 / SUSACK#	6	UI.			nas	13996.416	6246.876
AP13	Sx_EXIT_HOLDOFF# / GPP_A12 / BM_BUSY# / ISH_GP6	ndefine			lefined t		13082.016	6246.876
AP15	GPD4 / SLP_S3#	0.			inos		12167.616	6246.876
AP16	INTRUDER#			- ne			11253.216	6246.876
AP18	VSS			Yellin			10338.816	6246.876
AP2	GPP_F13 / EMMC_DATA0			Unc		1	19663.918	6781.8
AP20	VSS		iner			-d ui	9424.416	6246.876
AP21	DDR1_DQ[62]		dern			sine	8510.016	6246.876
AP22	DDR1_DQ[61]		Un			nde	7595.616	6246.876
AP23	VSS	ein ^e			6	0.	6681.216	6246.876
AP25	DDR1_DQ[55]	den			i stine		5766.816	6246.876
AP27	DDR1_DQ[52]	2011			Inde		4852.416	6246.876
AP28	VSS			_0	6		3938.016	6246.876
AP3	GPP_F15 / EMMC_DATA2			16/11			19013.678	6781.8
AP30	DDR1_DQ[47] / DDR1_DQ[31]			d uno-	DDR1_DQ[47]	DDR1_DQ[31]	3023.616	6246.876
AP32	VSS		Sinc			e co	2109.216	6246.876
AP33	DDR1_DQ[45] / DDR1_DQ[29]		unor		DDR1_DQ[45]	DDR1_DQ[29]	1194.816	6246.876
AP35	VSS		30 ×		2	UN	280.416	6246.876
AP37	DDR1_DQ[38] / DDR1_DQ[22]	Indefin			DDR1_DQ[38]	DDR1_DQ[22]	-633.984	6246.876
AP38	VSS	<u>,</u> d			un		-1548.384	6246.876
AP4	GPP_F12 / EMMC_CMD			00	ev.		18363.438	6781.8
AP40	DDR1_DQ[37] / DDR1_DQ[21]			unden	DDR1_DQ[37]	DDR1_DQ[21]	-2462.784	6246.876
AP42	VSS		-2. C	20			-3377.184	6246.876
AP43	DDR1_PAR		defill			tines	-4291.584	6246.876
AP45	DDR1_CKP[0]		, un			der.	-5205.984	6246.876
AP46	DDR1_CKP[1]		eu			d u'	-6120.384	6246.876
AP48	DDR1_MA[7] / DDR1_CAA[4] / DDR1_MA[7]	DDR1_MA[7]	DDR1_CAA[4]	DDR1_MA[7]	adefine		-7034.784	6246.876



ed undefined undefined Table 9-1. U/U-Quad Core Processor Ball List (Sheet 12 of 39)

	(intel)			odefine	U/U-Quad Co	re/YProcessor Ba	e co	1
	ofined		ed	UI		d un		
nu und	Table 9-1. U/U-0	Quad Core P	Processor Ba	II List (Shee	et 12 of 39)	stineu	1	r
Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- Interleaved (NIL)	X[um]	Y[um]
AP5	GPP_B21 / GSPI1_MISO	nder			76LILL		17654.016	6246.876
AP50	DDR1_MA[9] / DDR1_CAA[1] / DDR1_MA[9]	DDR1_MA[9]	DDR1_CAA[1]	DDR1_MA[9]	June		-7949.184	6246.876
AP52	DDR1_BA[2] / DDR1_CAA[5]/ DDR1_BG[0]	DDR1_BA[2]	DDR1_CAA[5]	DDR1_BG[0]			-8863.584	6246.876
AP53	DDR1_CKE[3]		ein ^e	Ð		àv	-9777.984	6246.876
AP55	DDR1_CKE[1]		den			fine	-10692.384	6246.876
AP56	MSM#		d un			Inde	-11606.784	6246.876
AP58	VSS	Sine			ed		-12521.184	6246.876
AP60	DDR1_DQ[26] / DDR0_DQ[58]	unde.			DDR1_DQ[26]	DDR0_DQ[58]	-13435.584	6246.876
AP61	DDR1_DQ[29] / DDR0_DQ[61]				DDR1_DQ[29]	DDR0_DQ[61]	-14349.984	6246.876
AP63	VSS			9em			-15264.384	6246.876
AP65	DDR1_DQ[18] / DDR0_DQ[50]			d une	DDR1_DQ[18]	DDR0_DQ[50]	-16178.784	6246.876
AP66	DDR1_DQ[21] / DDR0_DQ[53]		defill		DDR1_DQ[21]	DDR0_DQ[53]	-17093.184	6246.876
AP68	VSS		d un			nde	-18038.572	6331.966
AP7	GPP_B16 / GSPI0_CLK	242					16739.616	6246.876
AP70	VSS	de.			40111		-19257.772	6331.966
AP8	GPP_B17 / GSPI0_MISO	du.			unos		15825.216	6246.876
AR10	GPP_B5 / SRCCLKREQ0#			112	eo		14910.816	6897.116
AR11	VSS			der			13996.416	6897.116
AR13	GPP_A13 / SUSWARN# / SUSPWRDNACK			ed un			13082.016	6897.116
AR15	VSS		1641			sin ^{eo}	12167.616	6897.116
AR16	VSS		uno			der	11253.216	6897.116
AR18	DDR_RCOMP[0]	. *. 1	eo.			d un	10338.816	6897.116
AR20	VSS	deti			nia		9424.416	6897.116
AR21	DDR1_DQSP[7]	1 une			de.		8510.016	6897.116
AR22	DDR1_DQSN[7]	ner.			ed v.		7595.616	6897.116
AR23	VSS			10 Las			6681.216	6897.116
AR25	DDR1_DQSN[6]			unos			5766.816	6897.116
AR27	DDR1_DQSP[6]			neo			4852.416	6897.116
AR28	VSS		del				3938.016	6897.116
AR30	DDR1_DQ[46] / DDR1_DQ[30] DDR1_DQSP[5] /		red une		DDR1_DQ[46]	DDR1_DQ[30]	3023.616	6897.116
AR32	DDR1_DQSP[3]				2/2	6	2109.216	6897.116
AR33	DDR1_DQ[44] / DDR1_DQ[28]	ed un			DDR1_DQ[44]	DDR1_DQ[28]	1194.816	6897.116
	DDR1_DQ[44] / DDR1_DQ[28]	11.		tined unde	iner	Datasheet,	, Volume 1 of 2	led v.
	under.		inde	fine		Aefine		
sine			ed u.			y uno-		



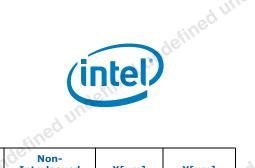
/YProcessor BallInformation U/U-Quad Core Processor Ball List (Sheet 13 of 39)

	U/U-Quad Core/YProce	ssor Bailinform	ation	indefine		intel			
Inde	Table 9-1. U/U-0	Quad Core P	rocessor Ba	Il List (Shee	et 13 of 39)	sined une			
Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- Interleaved (NIL)	X[um]	Y[um]	
AR35	VSS	. ndell			10fine		280.416	6897.11	
AR37	DDR1_DQ[39] / DDR1_DQ[23]	0.1			DDR1_DQ[39]	DDR1_DQ[23]	-633.984	6897.11	
AR38	DDR1_DQSP[4] / DDR1_DQSP[2]			defineo	DDR1_DQSP[4]	DDR1_DQSP[2]	-1548.384	6897.11	
AR40	DDR1_DQ[36] / DDR1_DQ[20]		6	uno	DDR1_DQ[36]	DDR1_DQ[20]	-2462.784	6897.11	
AR42	VSS		sinev			ed h.	-3377.184	6897.11	
AR43	VSS		JOE)			1.etine	-4291.584	6897.11	
AR45	VSS	60				nou	-5205.984	6897.11	
AR46	VSS	fine			ed		-6120.384	6897.11	
AR48	VSS	inde			Yellin		-7034.784	6897.11	
AR5	VSS			2	Un		17654.016	6897.11	
AR50	VSS			cine			-7949.184	6897.11	
AR52	VSS			der			-8863.584	6897.11	
AR53	VSS			Un			-9777.984	6897.11	
AR55	VSS		sine	P		.ed U	-10692.384	6897.11	
AR56	ZVM#		der.			i efine	-11606.784	6897.11	
AR58	VSS		, vi ·			anoc	-12521.184	6897.11	
AR60	DDR1_DQSP[3] / DDR0_DQSP[7]	define			DDR1_DQSP[3]	DDR0_DQSP[7]	-13435.584	6897.11	
AR61	DDR1_DQSN[3] / DDR0_DQSN[7]	d un			DDR1_DQSN[3]	DDR0_DQSN[7]	-14349.984	6897.11	
AR63	VSS			in ^e	2 ⁰ .		-15264.384	6897.11	
AR65	DDR1_DQSP[2] / DDR0_DQSP[6]			. Indein	DDR1_DQSP[2]	DDR0_DQSP[6]	-16178.784	6897.11	
AR66	DDR1_DQSN[2] / DDR0_DQSN[6]			9	DDR1_DQSN[2]	DDR0_DQSN[6]	-17093.184	6897.11	
AR68	DDR0_DQ[9]		ger.			stine	-18363.692	6945.37	
AR69	DDR0_DQ[13]		dui			Inoc	-19013.932	6945.37	
AR7	GPP_B18 / GSPI0_MOSI	-Sine			ed		16739.616	6897.11	
AR70	DDR0_DQ[8]	nder			16411		-19664.172	6846.31	
AR71	DDR0_DQ[12]	9 n.			uno		-20314.412	6846.31	
AR8	VSS				BO		15825.216	6897.11	
AT1	EMMC_RCOMP			detti			19989.038	7444.7	
AT10	GPP_B8 / SRCCLKREQ3#			dun			14910.816	7547.35	
AT11	GPP_B12 / SLP_S0#		Nija -	0-		. neò	13996.416	7547.35	
AT13	DRAM_RESET#		nde.			ACTIN	13082.016	7547.35	
AT15	GPD7 / RSVD		ed v.			, unc	12167.616	7547.35	
AT16	PROC_POPIRCOMP	ing,			e	D.	11253.216	7547.35	
AT18	DDR_RCOMP[1]	Inor			den		10338.816	7547.35	
AT2	VSS	ed			4 une		19338.798	7444.7	
	undefi			odefi			lefine		
	Datasheet, Volume 1 of 2			ned undefi		d undefined	unde 145	5	
						efine			
			d un.			nor			



ed undefined undefined Table 9-1. U/U-Quad Core Processor Ball List (Sheet 14 of 39)

		(intel)			sineu	U/U-Quad Co	ore/YProcessor Ba	llInformation	1
					nder			retitie	
		fine) V.		od un		
	Śn.	Table 9-1. U/U-0	Quad Core P	rocessor Ba	ll List (Shee	et 14 of 39)			
00	Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- Interleaved (NIL)	X[um]	Y[um]
F	AT20	VSS	deil		1	10/11/10	1	9424.416	7547.356
F	AT21	DDR1_DQ[59]	101		1	una	1	8510.016	7547.356
F	AT22	DDR1_DQ[56]				0	1	7595.616	7547.356
F	AT23	VSS			reting		1	6681.216	7547.356
F	AT25	DDR1_DQ[50]			unu			5766.816	7547.356
F	AT27	DDR1_DQ[49]		ne	P		-00	4852.416	7547.356
F	AT28	VSS		denn			tiner	3938.016	7547.356
	AT30	DDR1_DQ[43] / DDR1_DQ[27]	0	dun		DDR1_DQ[43]	DDR1_DQ[27]	3023.616	7547.356
	AT32	DDR1_DQSN[5] / DDR1_DQSN[3]	ndefin			DDR1_DQSN[5]	DDR1_DQSN[3]	2109.216	7547.356
	AT33	DDR1_DQ[40] / DDR1_DQ[24]	9			DDR1_DQ[40]	DDR1_DQ[24]	1194.816	7547.356
F	AT35	VSS			nn.	80	1	280.416	7547.356
F	AT37	DDR1_DQ[34] / DDR1_DQ[18]			undern	DDR1_DQ[34]	DDR1_DQ[18]	-633.984	7547.356
Γ	AT38	DDR1_DQSN[4] / DDR1_DQSN[2]			80	DDR1_DQSN[4]	DDR1_DQSN[2]	-1548.384	7547.356
┢	AT4	VSS		-yern,	+	<u> </u>	Filler	18363.438	7444.74
	AT40	DDR1_DQ[33] / DDR1_DQ[17]		ed un	†	DDR1_DQ[33]	DDR1_DQ[17]	-2462.784	7547.356
个	AT42	VSS	Activ		1	eine	1	-3377.184	7547.356
F	AT43	DDR0_ODT[1]	1 Une		1	ndel	1	-4291.584	7547.356
F	AT45	DDR0_ODT[0]	60	1	1	du.	1	-5205.984	7547.356
F	AT46	DDR0_WE#/ DDR0_CAB[2]/ DDR0_MA[14]	DDR0_WE#	DDR0_CAB[2]	DDR0_MA[14]			-6120.384	7547.356
F		DDR0_BA[1] / DDR0_CAB[6]/ DDR0_BA[1]	DDR0_BA[1]	DDR0_CAB[6]	DDR0_BA[1]		ed	-7034.784	7547.356
┢	AT5	TP6	<u> </u>	inde.	+	†	ACTIN	17654.016	7547.356
e	AT50	DDR0_MA[10] / DDR0_CAB[7]/ DDR0_MA[10]	DDR0_MA[10]	DDR0_CAB[7]	DDR0_MA[10]		ad unu-	-7949.184	7547.356
┢	AT52	DDR0_PAR	inde	1	+	- Yetin,	†	-8863.584	7547.356
┢	AT53	DDR0_CKP[0]	hed	1	+	1 y nn	†	-9777.984	7547.356
-	AT55	DDR0_CKP[1]	N 7	<u> </u>	<u> </u>	Ner.	†	-10692.384	7547.356
┢	AT56	VSS JUNO			nder	1	1	-11606.784	7547.356
┢	AT58	VSS			du.	1	1	-12521.184	7547.356
F	AT60	DDR1_DQ[30] / DDR0_DQ[62]		def	le-	DDR1_DQ[30]	DDR0_DQ[62]	-13435.584	7547.356
		DDR1_DQ[24] / DDR0_DQ[56]		ned un		DDR1_DQ[24]	DDR0_DQ[56]	-14349.984	7547.356
Y	AT63	VSS	101	N	<u> </u>	112	67	-15264.384	7547.356
	AT65	DDR1_DQ[22] / DDR0_DQ[54]	ed une			DDR1_DQ[22]	DDR0_DQ[54]	-16178.784	7547.356
		146	<i>III</i> ,		fined undef	inec	Datasheet,	, Volume 1 of 2	led un
		n,		ad unde	,		undefilt		



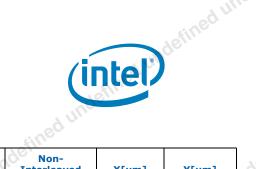
/YProcessor BallInformation U/U-Quad Core Processor Ball List (Sheet 15 of 39) Table 9-1.

Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- Interleaved (NIL)	X[um]	Y[um
AT66	DDR1_DQ[16] / DDR0_DQ[48]	Indelli			DDR1_DQ[16]	DDR0_DQ[48]	-17093.184	7547.3
AT68	VSS	<u> </u>		2	DIG.		-18038.572	7509.2
AT69	DDR0_DQSN[1]			sineu			-18688.812	7509.2
AT7	GPP_B6 /			.ndel.			16739.616	7547.3
AT70	SRCCLKREQ1# DDR0_DQSP[1]		0	01			-19339.052	7509.2
AT70	VSS		otine			ed -	-19339.032	7509.2
<u> </u>	GPP_B7 /		inde			definit		
AT8	SRCCLKREQ2#	ed			1	.00	15825.216	7547.3
AU1	SPI0_CS2#	defill			sineu		20314.158	8107.6
AU10	VSS	unv			der		14910.816	8197.5
AU11	GPP_A11 /PME#			_2	Un.		13996.416	8197.5
AU13	GPD0 / BATLOW#			sine.			13082.016	8197.5
AU15	VSS			nde.			12167.616	8197.5
AU16	PCH_OPIRCOMP					\u	11253.216	8197.5
AU18	DDR_RCOMP[2]		sinc			e ^o	10338.816	8197.5
AU2	SPI0_CS1#		unos			9611.	19663.918	8107.6
AU20	VSS	e			~	an.	9424.416	8197.5
AU21	DDR1_DQ[58]	Jefin.			tines.		8510.016	8197.5
AU22	DDR1_DQ[57]	unc			der		7595.616	8197.5
AU23	VDDQ	0			J. U.I.		6681.216	8197.5
AU25	DDR1_DQ[51]			fine			5766.816	8197.5
AU27	DDR1_DQ[48]			nde.			4852.416	8197.5
AU28	VDDQ			90			3938.016	8197.5
AU3	SPI0_CS0# DDR1_DQ[42] /		16/10			DDR1_DQ[26]	19013.678	8107.6
AU30	DDR1_DQ[26]		, unos		DDR1_DQ[42]	DDR1_DQ[20]	3023.616	8197.5
AU32	VSS		0			UI.	2109.216	8197.5
AU33	DDR1_DQ[41] / DDR1_DQ[25]	den			DDR1_DQ[41]	DDR1_DQ[25]	1194.816	8197.5
AU35	VDDQ	2400			nder		280.416	8197.5
AU37	DDR1_DQ[35] / DDR1_DQ[19]	<u>.</u>	<u> </u>	0.15	DDR1_DQ[35]	DDR1_DQ[19]	-633.984	8197.5
AU38	VSS			der.			-1548.384	8197.5
AU4	SPI0_IO3			dull			18363.438	8107.6
AU40	DDR1_DQ[32] / DDR1_DQ[16]		16tin	S	DDR1_DQ[32]	DDR1_DQ[16]	-2462.784	8197.5
AU42	VDDQ		, uno-			oder.	-3377.184	8197.5
AU43	DDR0_CS#[1]		60-			1 41,0	-4291.584	8197.5
AU45		Jerii	~		sine		5205 004	0107 5
	Datasheet, Volume 1 of 2	led und		ned undefil	ned unde	d undefined	undefine	d unde



B- Table 9-1. U/U-Quad Core Processor Ball List (Sheet 16 of 39)

	(intel)			define	U/U-Quad Co	re/YProcessor Ba	n eur	1
	and the			un			defili	
ind	Table 9-1. U/U-	Quad Core P	Processor Ba	ll List (Shee	et 16 of 39)	sined U.		
Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- Interleaved (NIL)	X[um]	Y[um]
AU46	DDR0_MA[13] / DDR0_CAB[0] / DDR0_MA[13]	DDR0_MA[13]	DDR0_CAB[0]	DDR0_MA[13]	undefine		-6120.384	8197.59
AU48	DDR0_CAS#/ DDR0_CAB[1]/ DDR0_MA[15]	DDR0_CAS#	DDR0_CAB[1]	DDR0_MA[15]	0		-7034.784	8197.59
AU5	TP5			A UNS			17654.016	8197.59
AU50	DDR0_RAS# / DDR0_CAB[3]/ DDR0_MA[16]	DDR0_RAS#	DDR0_CAB[3]	DDR0_MA[16]		efined v	-7949.184	8197.59
AU52	DDR0_BA[0] / DDR0_CAB[4]/ DDR0_BA[0]	DDR0_BA[0]	DDR0_CAB[4]	DDR0_BA[0]	ed	unoc	-8863.584	8197.59
AU53	DDR0_CKN[0]	nder			retin		-9777.984	8197.59
AU55	DDR0_CKN[1]	90			uno		-10692.384	8197.59
AU56	RSVD				,o		-11606.784	8197.59
AU58	VccGTx			-gein,			-12521.184	8197.59
AU60	DDR1_DQ[31] / DDR0_DQ[63]			dun	DDR1_DQ[31]	DDR0_DQ[63]	-13435.584	8197.59
AU61	DDR1_DQ[25] / DDR0_DQ[57]		Jefin		DDR1_DQ[25]	DDR0_DQ[57]	-14349.984	8197.59
AU63	VccGTx		, unas			dell	-15264.384	8197.59
AU65	DDR1_DQ[23] / DDR0_DQ[55]	1in	eo.		DDR1_DQ[23]	DDR0_DQ[55]	-16178.784	8197.59
AU66	DDR1_DQ[17] / DDR0_DQ[49]	d unor			DDR1_DQ[17]	DDR0_DQ[49]	-17093.184	8197.59
AU68	DDR0_DQ[11]	ec.			du		-18363.692	8146.79
AU69	DDR0_DQ[15]			in the second second	^C		-19013.932	8172.19
AU7	GPP_B10 / SRCCLKREQ5#			4 UNOP			16739.616	8197.59
AU70	DDR0_DQ[14]		<u> </u>	100		60	-19664.172	8172.19
AU71	DDR0_DQ[10]		der			1efine	-20314.412	8172.19
AU8	GPP_B9 / SRCCLKREQ4#		ed un			unos	15825.216	8197.59
AV1	VSS	Jeti			2016	0	20314.158	8827.51
AV2	SPI0_CLK	, unas			den		19364.198	8798.50
AV3	SPI0_MOSI	hea			dur		18688.558	8798.5
AV68	VSS	· · · · · · · · · · · · · · · · · · ·		i)	N ⁶⁵		-18028.92	8711.43
AV69	VSS	1		nde.			-19013.932	8901.17
AV70	VSS			ed v			-19664.172	8901.17
AV71	VSS		101	100		sine	-20314.412	8901.17
AW1	RSVD		inos			den	20314.158	9551.41
AW10	VSS		eq.			d un.	14752.828	9038.33
AW11	GPP_A8 / CLKRUN#	26	N		773	e	14143.228	9363.45
AW12	VSS	4 UNC			der		13565.124	9038.33
AW13	GPP_A0 / RCIN#	neu			dui		12995.148	9363.45
	148 undefined unde			tined unde	<i></i>	Datasheet	;, Volume 1 of 2	2
	d'un.		ed unde			undefin		



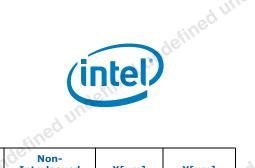
/YProcessor BallInformation U/U-Quad Core Processor Ball List (Sheet 17 of 39)

	U/U-Quad Core/YProce	SSOI DAIIINTOIN	اعدانا مک ^ا	C	ntel	,		
inde	Table 9-1. U/U-	Quad Core P	rocessor Ba	II List (Shee	et 17 of 39)	sined t		
Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- Interleaved (NIL)	X[um]	Y[um
AW14	VSS	ndell			10fine		12332.208	9038.3
AW15	SLP_LAN#	0.			JULO		11722.608	9363.4
AW16	VSS			tine ⁰			11144.504	9038.3
AW17	GPD11 / LANPHYPC			den.			10574.528	9363.4
AW18	VSS		2	un			9911.588	9038.3
AW2	SPI0_IO2		aneu			du.	19689.318	9362.4
AW20	I2S1_TXD		der.			afine	9301.988	9363.4
AW21	VSS	6	U			noc	8723.884	9038.3
AW22	HDA_RST# / I2S1_SCLK	sine			ed		8153.908	9363.4
AW23	VSS	nde			Jefill'		7465.568	9038.3
AW25	DDR0_DQ[59] / DDR1_DQ[43]				DDR0_DQ[59]	DDR1_DQ[43]	6828.028	9363.4
AW26	VSS			sine			6264.148	9038.3
AW27	DDR0_DQ[57] / DDR1_DQ[41]			. inde.	DDR0_DQ[57]	DDR1_DQ[41]	5601.208	9363.4
AW28	VSS					d UT	4987.798	9038.3
AW29	DDR0_DQ[51] / DDR1_DQ[35]		define		DDR0_DQ[51]	DDR1_DQ[35]	4374.388	9363.4
AW3	SPI0_MISO		, un			nde.	19039.078	9362.4
AW30	VSS	sine	<i></i>		Ó.		3711.448	9038.3
AW31	DDR0_DQ[49] /	ndell			DDR0_DQ[49]	DDR1_DQ[33]	3147.568	9363.4
	DDR1_DQ[33]	201			una			76,
AW32	VSS						2484.628	9038.3
AW33	DDR0_DQ[43] / DDR1_DQ[11]			detin	DDR0_DQ[43]	DDR1_DQ[11]	1847.088	9363.4
AW34	VSS			d un			1283.208	9038.3
AW35	DDR0_DQ[41] / DDR1_DQ[9]		fine		DDR0_DQ[41]	DDR1_DQ[9]	620.268	9363.4
AW36	VSS		Inde			defill	6.858	9038.3
AW37	DDR0_DQ[35] / DDR1_DQ[3]	Dia.	0		DDR0_DQ[35]	DDR1_DQ[3]	-606.552	9363.4
AW38	VSS	den			18fine		-1269.492	9038.3
AW39	DDR0_DQ[33] / DDR1_DQ[1]	edu			DDR0_DQ[33]	DDR1_DQ[1]	-1833.372	9363.4
AW41	VSS	~		0.is	e ^{co}		-2470.912	9038.3
AW42	DDR1_ODT[1]			dein.			-3108.452	9363.4
AW43	VSS	1		dui			-3672.332	9038.3
AW44	DDR1_RAS# / DDR1_CAB[3]/ DDR1_MA[16]	DDR1_RAS#	DDR1_CAB[3]	DDR1_MA[16]		stined	-4335.272	9363.4
AW45	VSS		ed ulli			unde	-4948.682	9038.3
AW46	DDR1_MA[10] / DDR1_CAB[7]/ DDR1_MA[10]	DDR1_MA[10]	DDR1_CAB[7]	DDR1_MA[10]	Aetine	Ò. Ŭ	-5562.092	9363.4
AW47	VSS	eo V.			d unu		-6162.802	9038.3
	Datasheet, Volume 1 of 2	, -		ned undefil	Ver.		define 149	, d
	Datasheet, Volume 1 of 2			ned		d undefined	Unc	-
			d un			under.		
11.		<i>C</i> _	ner			du.		



B- Table 9-1. U/U-Quad Core Processor Ball List (Sheet 18 of 39)

	(intel)			reting	u, u-quaa Co	re/YProcessor Ba		
	AUIT		-	una			9611	
	afine		ed			d ur	defin	
nı,	Table 9-1. U/U-0	Quad Core P	rocessor Ba	II List (Shee	t 18 of 39)	sinec	-	_
Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- Interleaved (NIL)	X[um]	Y[um]
AW48	RSVD	, del.			16tine		-6726.682	9363.450
AW49	VSS	A OFF			unos		-7355.332	9038.336
AW5	GPP_B14 / SPKR			9	0.		17780.508	8911.33
AW50	DDR0_ALERT#			16111			-7983.982	9363.45
AW51	VSS			una			-8547.862	9038.330
AW52	DDR0_MA[7] / DDR0_CAA[4] / DDR0_MA[7]	DDR0_MA[7]	DDR0_CAA[4]	DDR0_MA[7]		ofined	-9148.572	9363.456
AW53	VSS		Jun			mole	-9761.982	9038.336
AW54	DDR0_MA[12] / DDR0_CAA[6] / DDR0_MA[12]	DDR0_MA[12]	DDR0_CAA[6]	DDR0_MA[12]	Lefined		-10375.392	9363.456
AW55	VSS	90.			. uno		-11038.332	9038.336
AW56	DDR0_CKE[2]				,O		-11602.212	9363.45
AW57	VSS			Yeu			-12239.752	9038.33
AW59	DDR0_DQ[27] / DDR0_DQ[43]			ed une	DDR0_DQ[27]	DDR0_DQ[43]	-12877.292	9363.45
AW6	VSS		defil '			cipeu.	17130.268	9038.336
AW60	VSS		unos			dell	-13441.172	9038.330
AW61	DDR0_DQ[25] / DDR0_DQ[41]		ed -		DDR0_DQ[25]	DDR0_DQ[41]	-14104.112	9363.456
AW62	VSS	detti			Sine		-14717.522	9038.33
AW63	DDR0_DQ[18] /	4 Une			DDR0_DQ[18]	DDR0_DQ[34]	-15330.932	9363.456
AW64	DDR0_DQ[34] VSS	6			ed U.		-15993.872	9038.33
	DDR0_DQ[17] /			yetin	DDR0_DQ[17]	DDR0_DQ[33]	e ne	
AW65	DDR0_DQ[33]			June			-16557.752	9363.456
AW66	VSS			ler.		6	-17093.184	8900.414
AW67	DDR_VTT_CNTL		del.			eine	-18017.744	9370.56
AW68	RSVD		Un			nde	-18621.756	9622.02
AW69	RSVD		er.			d V.	-19266.916	9535.66
AW7	GPP_A23 / ISH_GP5	ger.			nin.		16563.848	9363.45
AW70	RSVD_TP	dun.			inde		-19684.746	10034.77
AW71	RSVD_TP	ne-			ed T		-20314.412	9551.41
AW8	VSS			Je ^{ff}			15985.744	9038.33
AW9	GPP_A9 / CLKOUT_LPC0 / ESPI_CLK			d unos			15415.768	9363.45
AY1	RSVD		c.	neu			20314.158	10201.65
AY11	GPP_A6 / SERIRQ		der	P		stine	14130.528	10013.69
AY12	GPP_A4 / LAD3 / ESPI_IO3		red une			a unde	13565.124	9688.57
AY13	GPP_A1 / LAD0 / ESPI_IO0	-96			All A	eu	12995.148	10013.69
AY15	_	dune			. mde.		11709.908	10013.69
	GPD1 / ACPRESENT	ine		tined undef	ined	Datasheet	:, Volume 1 of 2	led un
	d unde.		unde			adefin		
SING			ed			d Uni		



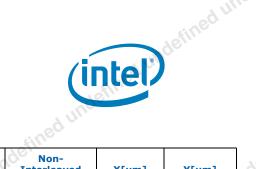
/YProcessor BallInformation U/U-Quad Core Processor Ball List (Sheet 19 of 39) Table 9-1.

Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- Interleaved (NIL)	X[um]	Y[um]
AY16	GPD10 / SLP_S5#	ndell			define		11144.504	9688.57
AY17	RSMRST#	0.			une		10574.528	10013.69
AY2	RSVD			⁰⁹ 0			19685	10034.2
AY20	I2S1_SFRM			dell'			9289.288	10013.69
AY21	HDA_SDI1 / I2S1_RXD		6	UL.		0,,	8723.884	9688.57
AY22	HDA_BLK / I2S0_SCLK		sines			ed v	8153.908	10013.69
AY25	DDR0_DQ[58] / DDR1_DQ[42]		unde		DDR0_DQ[58]	DDR1_DQ[42]	6828.028	10013.6
AY26	DDR0_DQSN[7] / DDR1_DQSN[5]	sineu			DDR0_DQSN[7]	DDR1_DQSN[5]	6264.148	9688.57
AY27	DDR0_DQ[56] / DDR1_DQ[40]	under			DDR0_DQ[56]	DDR1_DQ[40]	5601.208	10013.6
AY29	DDR0_DQ[50] / DDR1_DQ[34]	>		ed	DDR0_DQ[50]	DDR1_DQ[34]	4374.388	10013.6
AY3	RSVD			detin			19028.41	10027.9
AY30	DDR0_DQSP[6] / DDR1_DQSP[4] DDR0_DQ[48] /			une	DDR0_DQSP[6]	DDR1_DQSP[4]	3711.448	9688.57
AY31	DDR1_DQ[32] DDR0_DQ[42] /		ndefill		DDR0_DQ[42]	DDR1_DQ[10]	3147.568	10013.69
AY33 AY34	DDR1_DQ[10] DDR0_DQSN[5] /	sine	o U.		DDR0_DQSN[5]	DDR1_DQSN[1]	1847.088 1283.208	9688.57
AY35	DDR1_DQSN[1] DDR0_DQ[40] / DDR1_DQ[8]	under			DDR0_DQ[40]	DDR1_DQ[8]	620.268	10013.6
AY37	DDR1_DQ[3] DDR0_DQ[34] / DDR1_DQ[2]	D.		sine	DDR0_DQ[34]	DDR1_DQ[2]	-606.552	10013.69
AY38	DDR0_DQSP[4] / DDR1_DQSP[0]			undein	DDR0_DQSP[4]	DDR1_DQSP[0]	-1269.492	9688.57
AY39	DDR0_DQ[32] / DDR1_DQ[0]		a fine	0	DDR0_DQ[32]	DDR1_DQ[0]	-1833.372	10013.6
AY4	TP1		nde			defin	18274.284	10043.1
AY42	DDR1_CS#[1]		9			une	-3108.452	10013.6
AY43	DDR1_CAS#/ DDR1_CAB[1]/ DDR1_MA[15]	DDR1_CAS#	DDR1_CAB[1]	DDR1_MA[15]	definel	2	-3672.332	9688.57
AY44	DDR1_WE#/ DDR1_CAB[2]/ DDR1_MA[14]	DDR1_WE#	DDR1_CAB[2]	DDR1_MA[14]	ed uns		-4335.272	10013.6
AY46	DDR1_MA[1] / DDR1_CAB[8]/ DDR1_MA[1]	DDR1_MA[1]	DDR1_CAB[8]	DDR1_MA[1]			-5562.092	10013.6
AY47	DDR1_MA[2] / DDR1_CAB[5]/	DDR1_MA[2]	DDR1_CAB[5]	DDR1_MA[2]		stined	-6162.802	9688.57
AY48	DDR1_MA[2] DDR1_MA[5] / DDR1_CAA[0] /	DDR1_MA[5]	DDR1_CAA[0]	DDR1_MA[5]		d unde.	-6788.912	10013.69
AY5	DDR1_MA[5] GPP_B4 / CPU_GP3	ndeil.			1 etine		17664.684	9688.57
		ned un.		ned undefil	ned unoc		17004.004	d unde
	Datasheet, Volume 1 of 2			d under		undefined	ndefine	



ed undefined undefined Table 9-1. U/U-Quad Core Processor Ball List (Sheet 20 of 39)

	(intel)			undefineo	U/U-Quad Co	ore/YProcessor Ba		1
	101			nde			defill.	
	sine						defines	
hund	Table 9-1. U/U-	Quad Core P	Processor Ba	II List (Shee	et 20 of 39)	tineo	1	1
Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- Interleaved (NIL)	X[um]	Y[um]
AY50	DDR0_MA[0] / DDR0_CAB[9]/ DDR0_MA[0]	DDR0_MA[0]	DDR0_CAB[9]	DDR0_MA[0]	undefine		-7921.752	10013.696
AY51	DDR0_MA[2] / DDR0_CAB[5]/ DDR0_MA[2]	DDR0_MA[2]	DDR0_CAB[5]	DDR0_MA[2]	0.		-8547.862	9688.576
AY52	DDR0_MA[8] / DDR0_CAA[3] / DDR0_MA[8]	DDR0_MA[8]	DDR0_CAA[3]	DDR0_MA[8]		du	-9148.572	10013.696
AY54	DDR0_MA[14] / DDR0_CAA[9]/ DDR0_BG[1]	DDR0_MA[14]	DDR0_CAA[9]	DDR0_BG[1]		indefine	-10375.392	10013.696
AY55	DDR0_BA[2] / DDR0_CAA[5]/ DDR0_BG[0]	DDR0_BA[2]	DDR0_CAA[5]	DDR0_BG[0]	defined		-11038.332	9688.576
AY56	DDR0_CKE[3]	90.			, unc		-11602.212	10013.696
AY59	DDR0_DQ[31] / DDR0_DQ[47]			ein	DDR0_DQ[31]	DDR0_DQ[47]	-12877.292	10013.696
AY60	DDR0_DQSN[3] / DDR0_DQSN[5]			under	DDR0_DQSN[3]	DDR0_DQSN[5]	-13441.172	9688.576
AY61	DDR0_DQ[29] / DDR0_DQ[45]		nia	eq.	DDR0_DQ[29]	DDR0_DQ[45]	-14104.112	10013.696
AY63	DDR0_DQ[19] / DDR0_DQ[35]		, nuger.		DDR0_DQ[19]	DDR0_DQ[35]	-15330.932	10013.696
AY64	DDR0_DQSP[2] / DDR0_DQSP[4]	773	e o "		DDR0_DQSP[2]	DDR0_DQSP[4]	-15993.872	9688.576
AY65	DDR0_DQ[21] / DDR0_DQ[37]	under			DDR0_DQ[21]	DDR0_DQ[37]	-16557.752	10013.696
AY66	VSS	e		+	-d une	+	-17220.692	9688.576
AY67	DDR_VREF_CA			123	e	+	-17901.412	10013.696
AY68	DDR0_VREF_DQ	+		der.	+	+	-18535.396	10267.188
ATOO AY7	GPP_A22 / ISH_GP4			-9 m.	+		16551.148	10207.100
A17 AY71	VSS		73_	10 ⁻	+		-20314.412	10201.656
AT71 AY8	GPP_A18 / ISH_GP0				+	16/112	15985.744	9688.576
AY8 AY9	GPP_A10 / CLKOUT_LPC1		ned UN			d una-	15985.744	10013.696
B10	VSS	deil		+	Alle	() ⁻	14988.794	-10338.816
B10 B11	RSVD	1 June			nde.	+	14313.154	-10663.936
B13	USB3_2_TXN / SSIC_TXN	Ner.		ci	nedu		13186.41	-10663.936
B14	VSS			~96J	<u> </u>	+	12510.77	-10338.816
B15	USB3_3_TXN			dui	+	+	11835.13	-10663.936
B17	PCIE1_TXN / USB3_5_TXN		101	ner		ane ^e	10708.386	-10663.936
B18	VSS			+	+	defini	10032.746	-10338.816
B19	PCIE4_TXN		ned v		+	200-	9357.106	-10663.936
B19 B2	RSVD	20		<u> </u>	275	ev	19831.558	-10831.576
		, unas		<u> </u>	-dell'			
B21	PCIE7_TXN / SATA0_TXN	med			ed une		8230.362	-10663.936
	inde			26	in.		1iii	1eu
	SATAO_TXN			fined unde		Datasheet	, Volume 1 of 2	2
	una		nde			Aefin		
sine			ed u'			, uno-		



/YProcessor BallInformation U/U-Quad Core Processor Ball List (Sheet 21 of 39)

inde	tined unoc	essor BallInform Quad Core P	ed l	Ind ^{efitt}	et 21 of 39)	fined un	ntel	
Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- Interleaved (NIL)	X[um]	Y[um]
B22	VSS	ndeili			1.efine		7554.722	-10338.8
B23	PCIE9_TXN	0		÷	JULO		6879.082	-10663.9
B25	PCIE12_TXP / SATA2_TXP			ineo			5752.338	-10663.9
B26	CSI2_CLKN3			dein			5076.698	-10338.8
B27	 CSI2_DP10		2	UN		01.	4401.058	-10663.9
B29	 CSI2_DP8		sinec			. ed V.	3274.314	-10663.9
B3	RSVD		nde''			1 of inc	19196.558	-10679.1
B30	VSS	6.	JI.			nac	2598.674	-10338.8
B31	CSI2_DP6	-SUUS-			ed	P	1923.034	-10663.9
B33	CSI2_DP7	'UGE.			1/15		796.29	-10663.9
B33	VSS				Uno-		120.65	-10338.8
вз4 В36	CSI2_DP0						-554.99	-10558.8
	CSI2_DP3			Jeili -				-10663.9
B38	VSS			unor			-1681.734	
B39						LU S	-2357.374	-10338.8
B40	CLKOUT_PCIE_N4		Jetti,			sine.	-3033.014	-10663.9
B42	CLKOUT_PCIE_N1		unu			.~9e/.	-4159.758	-10663.9
B44	VSS	ane l			6-	01.	-4835.398	-10338.8
B45	EDP_TXP[2]	ein			ines.		-5511.038	-10663.9
B47	EDP_TXP[3]	une			der		-6637.782	-10663.9
B48	VSS	0			d UN		-7313.422	-10338.8
B5	SYS_RESET#			nine			18048.478	-10663.9
B50	DDI2_TXP[2]			de.			-7989.062	-10663.9
B52	EDP_DISP_UTIL			d'u'			-9115.806	-10663.9
B53	VSS		fine			ed '	-9791.446	-10338.8
B54	BPM#[2]		nde			16/11/	-10467.086	-10663.9
B56	PCH_JTAG_TCK	0	,d V.			unc	-11593.83	-10663.9
B58	VSS	a fin	~		e C		-12269.47	-10338.8
B59	PROC_TRST#	inoc			detin		-12945.11	-10663.9
B6	SYS_PWROK	60			a une		17466.818	-10338.8
B61	PROC_TCK			γ_{i5}	60.		-14071.854	-10663.9
B62	VSS			gerr			-14747.494	-10338.8
B63	VIDALERT#			d un			-15423.134	-10663.9
B65	VCCST_PWRGD		072	30		bo	-16549.878	-10663.9
B66	VSS		der			stine	-17225.518	-10338.8
B67	CFG[1]		duit			Inor	-17901.158	-10663.9
B69	RSVD	Nija_	0		_0	0	-19035.014	-10684.
B7	GPP_D4 / FLASHTRIG	, de,			10ftne		16791.178	-10663.9
B70	RSVD	~d~~	ned undefil		Inor		-19685.254	-10684.

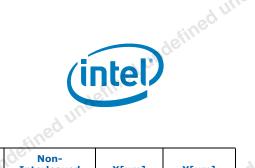
define	Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- Interleaved (NIL)	X[um]	Y[um]
<u>uc</u> .	B71	VSS	nder			retine		-20314.412	-10851.896
	B9	GPP_E12 / USB2_OC3#) ().			une		15664.434	-10663.936
	BA1	VSS			e	0		20314.158	10851.896
	BA10	VSS			9ern.			14752.828	10257.536
	BA11	GPP_A14 / SUS_STAT#/ ESPI_RESET#			dune		ن _	14188.948	10663.936
	BA12	GPP_A5 / LFRAME# / ESPI_CS#		defill			lefine C	13565.124	10338.816
file	BA13	GPP_A2 / LAD1 / ESPI_IO1	e	d U.		6-	unos	12995.148	10663.936
INOC	BA14	VSS	defin			4inec		12332.208	10257.536
	BA15	GPD3 / PWRBTN#	, un			de.		11768.328	10663.936
	BA16	GPD5 / SLP_S4#				00.		11144.504	10338.816
	BA17	GPD8 / SUSCLK			inite and the second	<i></i>		10574.528	10663.936
	BA18	VSS			inoc			9911.588	10257.536
	BA2	VSS			60			19685	10684.51
	BA20	PCH_PWROK HDA SDI0/ I2S0 RXD		Xe ⁽¹¹⁾			eineu	9347.708	10663.936
	BA21	HDA_SDIO/ I2S0_KXD HDA_SYNC / I2S0_SFRM		, uno				8723.884	10338.816
i esti	BA22	VSS	2.5	20			UI.	8153.908	10663.936
unoc	BA23 BA25	DDR0_DQ[62] / DDR1_DQ[46]	Indefin			DDR0_DQ[62]	DDR1_DQ[46]	7465.568 6828.028	10257.536 10663.936
	BA26	DDR0_DQSP[7] / DDR1_DQSP[5]	ed			DDR0_DQSP[7]	DDR1_DQSP[5]	6165.088	10338.816
	BA27	DDR0_DQ[61] / DDR1_DQ[45]			ndefil	DDR0_DQ[61]	DDR1_DQ[45]	5502.148	10663.936
	BA28	VSS			du			4987.798	10257.536
	BA29	DDR0_DQ[54] / DDR1_DQ[38]		defi		DDR0_DQ[54]	DDR1_DQ[38]	4473.448	10663.936
	BA3	RSVD		d'un.			inde	19034.76	10684.51
inde	BA30	DDR0_DQSN[6] / DDR1_DQSN[4]	Jefi	165		DDR0_DQSN[6]	DDR1_DQSN[4]	3810.508	10338.816
	BA31	DDR0_DQ[53] / DDR1_DQ[37]	ed und			DDR0_DQ[53]	DDR1_DQ[37]	3147.568	10663.936
	BA32	VSS	<u>no</u>			AeO .		2484.628	10257.536
	BA33	DDR0_DQ[46] / DDR1_DQ[14]			ndet	DDR0_DQ[46]	DDR1_DQ[14]	1847.088	10663.936
	BA34	DDR0_DQSP[5] / DDR1_DQSP[1]			ned u.	DDR0_DQSP[5]	DDR1_DQSP[1]	1184.148	10338.816
	BA35	DDR0_DQ[45] / DDR1_DQ[13]		ndei		DDR0_DQ[45]	DDR1_DQ[13]	521.208	10663.936
	BA36	VSS		Led T			un	6.858	10257.536
d und	BA37	DDR0_DQ[38] / DDR1_DQ[6]	ndef	<i>U</i> .		DDR0_DQ[38]	DDR1_DQ[6]	-507.492	10663.936
0	BA38	DDR0_DQSN[4] / DDR1_DQSN[0]	ned U			DDR0_DQSN[4]	DDR1_DQSN[0]	-1170.432	10338.816
		154	12.		tined unde	times		Volume 1 of 2	led -
	efiner			med uno			d undefine		

ndefined undefine

U/U-Quad Core/YProcessor BallInformation



(intel) ed undefine



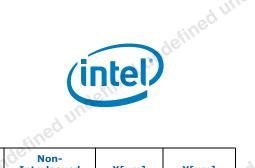
/YProcessor BallInformation U/U-Quad Core Processor Ball List (Sheet 23 of 39) Table 9-1.

Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- Interleaved	X[um]	Y[um
BA39	DDR0_DQ[37] /	define			DDR0_DQ[37]	(NIL) DDR1_DQ[5]	1022 272	10663.0
	DDR1_DQ[5]	711-			nde		-1833.372	10663.9
BA4	RSVD			60	0		18365.724	10689.3
BA41	VSS			sinc			-2470.912	10257.
BA42	DDR1_ODT[0]			mar			-3108.452	10663.9
BA43	DDR1_MA[13] / DDR1_CAB[0] / DDR1_MA[13]	DDR1_MA[13]	DDR1_CAB[0]	DDR1_MA[13]		uned un	-3771.392	10338.8
BA44	DDR1_BA[1] / DDR1_CAB[6]/ DDR1_BA[1]	DDR1_BA[1]	DDR1_CAB[6]	DDR1_BA[1]		nden	-4434.332	10663.9
BA45	VSS	i ofine			ed		-4948.682	10257.5
BA46	DDR1_MA[0] / DDR1_CAB[9]/ DDR1_MA[0]	DDR1_MA[0]	DDR1_CAB[9]	DDR1_MA[0]	undefili		-5463.032	10663.9
BA47	DDR1_MA[0]			4 net	1		-6125.972	10338.8
BA48	DDR1_MA[6] / DDR1_CAA[2] / DDR1_MA[6]	DDR1_MA[6]	DDR1_CAA[2]	DDR1_MA[6]			-6788.912	10663.9
BA49	VSS		e'ne'				-7355.332	10338.8
BA5	GPP_B3 / CPU_GP2		JOE''			interine	17715.484	10625.8
BA50	DDR0_MA[3]		9. 7			1005	-7921.752	10663.9
BA51	DDR0_MA[5] / DDR0_CAA[0] / DDR0_MA[5]	DDR0_MA[5]	DDR0_CAA[0]	DDR0_MA[5]	refined	<u>~</u>	-8584.692	10338.8
BA52	DDR0_MA[6] / DDR0_CAA[2] / DDR0_MA[6]	DDR0_MA[6]	DDR0_CAA[2]	DDR0_MA[6]	d une		-9247.632	10663.9
BA53	VSS			dein			-9761.982	10257.5
BA54	DDR0_MA[11] / DDR0_CAA[7] / DDR0_MA[11]	DDR0_MA[11]	DDR0_CAA[7]	DDR0_MA[11]		ed l	-10276.332	10663.9
BA55	DDR0_MA[15] / DDR0_CAA[8]/ DDR0_ACT#	DDR0_MA[15]	DDR0_CAA[8]	DDR0_ACT#		Indefine	-10939.272	10338.8
BA56	DDR0_CKE[0]	nip.	9		ed		-11602.212	10663.9
BA57	VSS	inds.			Jetill		-12239.752	10257.
BA59	DDR0_DQ[30] / DDR0_DQ[46]	50 M.			DDR0_DQ[30]	DDR0_DQ[46]	-12877.292	10663.9
BA6	VSS			afin a	5		17173.448	10257.
BA60	DDR0_DQSP[3] / DDR0_DQSP[5]			ed unor	DDR0_DQSP[3]	DDR0_DQSP[5]	-13540.232	10338.8
BA61	DDR0_DQ[24] / DDR0_DQ[40]		10fil		DDR0_DQ[24]	DDR0_DQ[40]	-14203.172	10663.9
BA62	VSS		ince			deri	-14717.522	10257.
BA63	DDR0_DQ[22] / DDR0_DQ[38]	line	ed		DDR0_DQ[22]	DDR0_DQ[38]	-15231.872	10663.9
BA64	DDR0_DQSN[2] / DDR0_DQSN[4]	inde			DDR0_DQSN[2]	DDR0_DQSN[4]	-15894.812	10338.
	Datasheet, Volume 1 of 2	160		ned undefit	ned U.	d undefined	undefine	d und



ed undefined undefined Table 9-1. U/U-Quad Core Processor Ball List (Sheet 24 of 39)

	(intel)			1efine	U/U-Quad Co	re/YProcessor Ba	allInformation	ו
	- UI			uno			dell.	
	erine		iner	S		d un		
nu un	Table 9-1. U/U-0	Quad Core P	rocessor Ba	all List (She	et 24 of 39)	sines	1	1
Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- Interleaved (NIL)	X[um]	Y[um]
BA65	DDR0_DQ[20] / DDR0_DQ[36]	Inder			DDR0_DQ[20]	DDR0_DQ[36]	-16557.752	10663.93
BA66	VSS				JUNC		-17220.692	10338.81
BA67	DDR1_VREF_DQ			1012			-17901.412	10663.93
BA68	RSVD_TP			deit			-19034.506	10685.01
BA7	GPP_A21 / ISH_GP3			0.011			16609.568	10663.93
BA70	RSVD_TP		Sin			eo l	-19684.746	10685.01
BA71	VSS		inde			retin	-20314.412	10851.89
BA8	GPP_A19 / ISH_GP1	-	9		2	JULE	15985.744	10338.81
BA9	GPP_A17 / SD_PWR_EN# / ISH_GP7	indefin			defineo		15415.768	10663.93
BB10	DCPRTC	ò			JUNY		14752.828	10989.05
BB11	GPP_A7 / PIRQA#			275	100		14188.948	11314.17
BB13	GPP_A3 / LAD2 / ESPI_IO2			ndeit			12995.148	11314.17
BB14	VCCRTC			60 V.			12332.208	10989.05
BB15	WAKE#		1611			^O 90is	11768.328	11314.17
BB17	GPD9 / SLP_WLAN#		, uno-			dell	10574.528	11314.17
BB18	VSS		8 0			101	9911.588	10989.05
BB2	RSVD	detti			Sinc	<i></i>	19851.878	11314.17
BB20	DSW_PWROK	d Une			nder		9347.708	11314.17
BB22	HDA_SDO / I2S0_TXD	e			0		8153.908	11314.17
BB23	VDDQ				100		7465.568	10907.77
BB25	DDR0_DQ[63] / DDR1_DQ[47]			d unos	DDR0_DQ[63]	DDR1_DQ[47]	6828.028	11314.17
BB26	VSS		(i)			ed	6165.088	10989.05
BB27	DDR0_DQ[60] / DDR1_DQ[44]		unde.		DDR0_DQ[60]	DDR1_DQ[44]	5502.148	11314.17
BB29	DDR0_DQ[55] / DDR1_DQ[39]		leo		DDR0_DQ[55]	DDR1_DQ[39]	4473.448	11314.17
BB3	TP2	nde			Aeth.		19201.638	11314.17
BB30	VSS	edv			un		3810.508	10989.05
BB31	DDR0_DQ[52] / DDR1_DQ[36]	/ ~			DDR0_DQ[52]	DDR1_DQ[36]	3147.568	11314.17
BB32	VDDQ			nde			2484.628	10907.77
BB33	DDR0_DQ[47] / DDR1_DQ[15]			hed u	DDR0_DQ[47]	DDR1_DQ[15]	1847.088	11314.17
BB34	VSS		. Ye			sine	1184.148	10989.05
BB35	DDR0_DQ[44] / DDR1_DQ[12]		d un		DDR0_DQ[44]	DDR1_DQ[12]	521.208	11314.17
BB37	DDR0_DQ[39] / DDR1_DQ[7]	-9e	IL.		DDR0_DQ[39]	DDR1_DQ[7]	-507.492	11314.17
BB38		dune			inde.		-1170.432	10989.05
	vss 156 undefined undef	Ines		stined und	afined	Datasheet	, Volume 1 of 2	ned une
	d une		d unde			indefin		



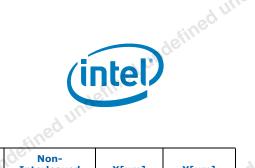
/YProcessor BallInformation U/U-Quad Core Processor Ball List (Sheet 25 of 39)

	od under	essor BallInforn		Indefine		intel			
inde	Table 9-1. U/U-	Quad Core P	Processor Ba	Il List (Shee	et 25 of 39)	sined une			
Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- Interleaved (NIL)	X[um]	Y[um]	
BB39	DDR0_DQ[36] / DDR1_DQ[4]	Inder			DDR0_DQ[36]	DDR1_DQ[4]	-1833.372	11314.1	
BB4	RSVD			À	UNC		18551.398	11314.1	
BB41	VDDQ			sineu	<u>}</u>		-2470.912	10907.7	
BB42	DDR1_CS#[0]			de			-3108.452	11314.1	
BB43	VSS		6	0.		. un	-3771.392	10989.0	
BB44	DDR1_BA[0] / DDR1_CAB[4]/ DDR1_BA[0]	DDR1_BA[0]	DDR1_CAB[4]	DDR1_BA[0]		defineo	-4434.332	11314.1	
BB46	DDR1_MA[3]	d	<u>.</u>		5.0	00	-5463.032	11314.1	
BB47	VDDQ	16/11/2			cin ^{eo}		-6125.972	10989.0	
BB48	DDR1_MA[8] / DDR1_CAA[3] / DDR1_MA[8]	DDR1_MA[8]	DDR1_CAA[3]	DDR1_MA[8]	unden		-6788.912	11314.1	
BB5	TP4			sine			17785.588	11314.1	
BB50	DDR0_MA[1] / DDR0_CAB[8]/ DDR0_MA[1]	DDR0_MA[1]	DDR0_CAB[8]	DDR0_MA[1]			-7921.752	11314.1	
BB51	VDDQ		sine	<i>v</i>		ed v	-8584.692	10989.0	
BB52	DDR0_MA[4]		nde.			reting	-9247.632	11314.1	
BB54	DDR0_MA[9] / DDR0_CAA[1] / DDR0_MA[9]	DDR0_MA[9]	DDR0_CAA[1]	DDR0_MA[9]	ned	JUG	-10276.332	11314.1	
BB55	VSS	Inde			derini		-10939.272	10989.0	
BB56	DDR0_CKE[1]	0			A UNC		-11602.212	11314.1	
BB57	VccGTx			ein ^e	3		-12239.752	10907.7	
BB59	DDR0_DQ[26] / DDR0_DQ[42]			nder	DDR0_DQ[26]	DDR0_DQ[42]	-12877.292	11314.1	
BB6	VSS			Ò		21	17173.448	10989.0	
BB60	VSS		<i>yetin</i>			sineu	-13540.232	10989.0	
BB61	DDR0_DQ[28] / DDR0_DQ[44]		d une		DDR0_DQ[28]	DDR0_DQ[44]	-14203.172	11314.1	
BB63	DDR0_DQ[23] / DDR0_DQ[39]	defin			DDR0_DQ[23]	DDR0_DQ[39]	-15231.872	11314.1	
BB64	VSS	JUTT			nde		-15894.812	10989.0	
BB65	DDR0_DQ[16] / DDR0_DQ[32]	e			DDR0_DQ[16]	DDR0_DQ[32]	-16557.752	11314.1	
BB66	VccGTx			deri			-17220.692	10989.0	
BB67	VSS			dull			-17901.412	11314.1	
BB68	RSVD_TP		2/3	6		69	-18551.652	11314.1	
BB69	RSVD_TP		nder			Lefine	-19201.892	11314.1	
BB7	GPP_A20 / ISH_GP2		du			uno	16609.568	11314.1	
BB70	VSS	il.			2	0	-19852.132	11314.1	
BB9	GPP_A16 / SD_1P8_SEL	nov			detti		15415.768	11314.1	
	VSS	<u>d</u> .		ned undefi	, une		20314.158	-10348.9	



B-Table 9-1. U/U-Quad Core Processor Ball List (Sheet 26 of 39)

, un	Table 9-1. U/U-C	Quad Core P	rocessor Ba	all List (She	et 26 of 39)	1efines	1	1
Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- Interleaved (NIL)	X[um]	Y[um]
C11	RSVD	uder.			1efine		14313.154	-10013.69
C12	RSVD) Or			unos		13749.782	-10338.81
C13	USB3_1_TXN				<u>}0</u>		13186.41	-10013.69
C15	USB3_4_TXN			Yeun			11835.13	-10013.69
C16	PCIE2_TXP / USB3_6_TXP			June			11271.758	-10338.81
C17	PCIE3_TXP		nia.	30.		60	10708.386	-10013.69
C19	PCIE5 TXN		, del.			1 of the	9357.106	-10013.69
C2	RSVD		0.01.			inge	19679.158	-10196.57
C20	PCIE6_TXP	AIR			ed		8793.734	-10338.81
C21	PCIE8_TXP / SATA1A_TXP	d unde			indefill		8230.362	-10013.69
C23	PCIE10_TXP			_	0		6879.082	-10013.69
C24	PCIE11_TXP / SATA1B_TXP			defin			6315.71	-10338.81
C25	VSS			du			5752.338	-10013.69
C27	CSI2_DN11		113			ed	4401.058	-10013.69
C28	CSI2_DN9		nde			16th	3837.686	-10338.81
C29	CSI2_CLKN2		<u>,</u> d			une	3274.314	-10013.69
C31	CSI2_DN4	iefin			ine'	0	1923.034	-10013.69
C32	CSI2_CLKN1	inor			den		1359.662	-10338.81
C33	CSI2_DN5	ed			4 Un		796.29	-10013.69
C36	CSI2_DN2			61	0 ^{eu}		-554.99	-10013.69
C37	CSI2_CLKN0			der			-1118.362	-10338.81
C38	CSI2_DN1			d un.			-1681.734	-10013.69
C4	RSVD		13_	n ^{e-}		d	18614.898	-10336.27
C40	CLKOUT_PCIE_P3		nder.			1erino	-3033.014	-10013.69
C41	CLKOUT_PCIE_P2		du.			una	-3596.386	-10338.81
C42	CLKOUT_PCIE_P0	afil				0	-4159.758	-10013.69
C45	EDP_TXP[1]	-unor			defin		-5511.038	-10013.69
C46	EDP_TXP[0]	ed			J Ulli-		-6074.41	-10338.83
C47	EDP_TXN[0]			6	Ner.		-6637.782	-10013.69
C5	VSS						18048.478	-10013.69
C50	DDI2_TXN[0]			du'			-7989.062	-10013.69
C51	DDI2_TXP[3]			ine		e	-8552.434	-10338.81
C52	DDI2_TXN[1]		, unde			defini	-9115.806	-10013.69
C54	RSVD		hed y			2 un	-10467.086	-10013.69
C55	BPM#[0]	- Xe ^r	<i>1</i> ,		202	eu	-11030.458	-10338.8
C56	BPM#[3]	1 UNOS			- dell.		-11593.83	-10013.69
C59	PCH_JTAG_TMS	ined -			Loco Ulli		-12945.11	-10013.6
	158			afined unde	SUL.		1011	ner.
	158			du.		Datasheet	, Volume 1 of 2	2
	yer.							



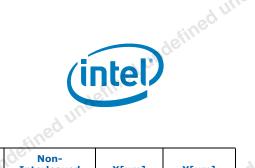
/YProcessor BallInformation U/U-Quad Core Processor Ball List (Sheet 27 of 39)

. de				Indefin		<u> </u>	ntel	
<i>.............</i>	Table 9-1. U/U-C	Quad Core P	rocessor Ba	ll List (Shee	et 27 of 39)	sined un.		
Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- Interleaved (NIL)	X[um]	Y[um]
C60	PROC_TMS	.nde.			16fine		-13508.482	-10338.8
C61	PCH_TRST#	01		*	uno		-14071.854	-10013.6
C63	THERMTRIP#			eo			-15423.134	-10013.6
C64	PROC_SELECT#			Jelli			-15986.506	-10338.8
C65	PROCHOT#			unu		~	-16549.878	-10013.6
C67	CFG[7]		ine ^o			d un	-18485.104	-10299.4
C68	CFG[5]		detti			sinet	-18622.264	-9621.5
C7	RSVD	2	Une			nde.	16791.178	-10013.6
C70	RSVD	ei neu			9.0		-19685.254	-10034.2
C71	RSVD	der			fine		-20314.412	-10201.6
C8	GPP_D18 / DMIC_DATA1	<i>viv</i>			Inde		16227.806	-10338.8
C9	GPP_E10 / USB2_OC1#	-		0			15664.434	-10013.6
D1	RSVD			10fine			20314.158	-9698.73
D10	VSS			INOC			14988.794	-9322.8
D11	VSS		ec			d U	14313.154	-9363.4
D12	RSVD		Actin			eineu	13749.782	-9688.5
D13	USB3_1_TXP		uno			dell	13186.41	-9363.45
D14	VSS	ine e	>		6-	<u>(1)</u>	12510.77	-9322.8
D15	USB3_4_TXP	det.			sines		11835.13	-9363.4
D16	PCIE2_TXN / USB3_6_TXN	d Une			under		11271.758	-9688.57
	PCIE3_TXN			in ne	<u>, 0</u>		10708.386	-9363.45
D18	VSS			Jer.			10032.746	-9322.8
D19	PCIE5_TXP			1 Uno			9357.106	-9363.4
D20	PCIE6_TXN		ei n ^e	0		0	8793.734	-9688.57
D21	PCIE8_TXN / SATA1A_TXN		undein			define	8230.362	-9363.4
D22	VSS		,Ò		2	Un	7554.722	-9322.8
D23	PCIE10_TXN	Aerit.			sinet		6879.082	-9363.4
D24	PCIE11_TXN / SATA1B_TXN	d une			under		6315.71	-9688.5
D25	VSS	9			e ^o		5752.338	-9363.4
D26	VSS			Yelli			5076.698	-9322.8
D27	CSI2_DP11			1 Uni			4401.058	-9363.4
D28	CSI2_DP9		0.55	80		6	3837.686	-9688.5
D29	CSI2_CLKP2		dein		1	fine	3274.314	-9363.4
D3	RSVD		dun		1	nos	19338.798	-9608.3
D30	VSS	212	6		0	3	2598.674	-9322.8
D31	CSI2_DP4	der			1. STIPE		1923.034	-9363.4
D32	CSI2_CLKP1	-d vii	ned undefil		. Inde		1359.662	-9688.5



ed undefined undefined Table 9-1. U/U-Quad Core Processor Ball List (Sheet 28 of 39)

	(intel)			retime	u/u-quad Co	re/YProcessor Ba	antinormation	,
	AU.			uno			9e11.	
	efine		ined			d ul		
nu	Table 9-1. U/U-Q	Quad Core P	rocessor Ba	Il List (She	et 28 of 39)	Ainec	1	1
Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- Interleaved (NIL)	X[um]	Y[um]
D33	CSI2_DP5	ndell			18fth		796.29	-9363.45
D34	VSS	, Uii			unos		120.65	-9322.81
D36	CSI2_DP2				jo -		-554.99	-9363.45
D37	CSI2_CLKP0			Yelli			-1118.362	-9688.57
D38	CSI2_DP1			Une			-1681.734	-9363.45
D39	VSS		an ^e	2		6	-2357.374	-9322.81
D4	RSVD		detti			Since	18690.59	-9668.5
D40	CLKOUT_PCIE_N3		y Une			nder	-3033.014	-9363.45
D41	CLKOUT_PCIE_N2	cine			6	0.	-3596.386	-9688.57
D42	CLKOUT_PCIE_N0	der			afine		-4159.758	-9363.45
D44	VSS	d UN			Inde		-4835.398	-9322.81
D45	VSS			_	e à l'		-5511.038	-9363.45
D46	EDP_TXN[1]			1 ing			-6074.41	-9688.57
D47	VSS			inos			-6637.782	-9363.45
D48	VSS			eò .		2	-7313.422	-9322.81
D5	RSVD		ACTIN			ein ^{eu}	18090.388	-9363.45
D50	DDI2_TXP[0]		, una			dell	-7989.062	-9363.45
D51	DDI2_TXN[3]		80			1 vili	-8552.434	-9688.57
D52	DDI2_TXP[1]	Jeil.			Sine		-9115.806	-9363.45
D53	VSS	JUNE			nder		-9791.446	-9322.81
D54	RSVD	20°			d'u		-10467.086	-9363.45
D55	BPM#[1]			il)	0		-11030.458	-9688.57
D56	PROC_PRDY#			. noe			-11593.83	-9363.45
D58	VSS			00		2	-12269.47	-9322.81
D59	PCH_JTAG_TDI		1811			cin ^{ec}	-12945.11	-9363.45
D6	VSS		inoc			der.	17441.418	-9322.81
D60	PROC_TDI		led L			2 UNC	-13508.482	-9688.57
D61	PROC_PREQ#	Jett			nia		-14071.854	-9363.45
D62	VSS	, uno			001		-14747.494	-9322.81
D63	CATERR#	100			dull		-15423.134	-9363.45
D64	VIDSOUT			2	ine-		-15986.506	-9688.57
D65	CFG[2]			,nde	-		-16549.878	-9363.45
D66	VSS			ed un			-17225.518	-9322.81
D67	CFG[3]			n.e		0	-17898.618	-10013.6
D68	CFG[6]		. Inde			Yeth	-19267.424	-9535.1
D69	VSS		eo U.			y une	-18561.812	-8971.02
D7	GPP_D20 / DMIC_DATA0	10	11-			(e ⁰	16791.178	-9363.45
		, unos			detti		-20314.412	-9551.41
- / -		ned	I	<u> </u>	d une		2001 1112	
	RSVD 160	.	ined unde	20	fine			ned -
	160			4 UNU		Datasheet	, Volume 1 of 2	2
	define			fineu			ed un	
	un		nde			76 <i>tiu</i>		
			du					



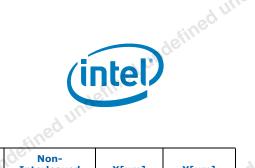
/YProcessor BallInformation U/U-Quad Core Processor Ball List (Sheet 29 of 39)

Ball #	Table 9-1. U/U-C	DDR3L	LPDDR3	II List (Shee DDR4	Interleaved (IL)	Non- Interleaved (NIL)	X[um]	Y[um]
D8	GPP_D17 / DMIC_CLK1	defili			enneu	(NIL)	16227.806	-9688.5
D9	GPP_E11 / USB2_OC2#	<u>.</u>			INGE		15664.434	-9363.4
E1	RSVD			eq.			20314.158	-9039.8
E10	USB3_4_RXN			Jeting			14910.816	-8591.2
E11	VSS			uno		~	13996.416	-8591.2
E13	CSI2_COMP		cineo.			dui	13082.016	-8591.2
E15	VSS		deit			fines	12167.616	-8591.2
E16	PCIE5_RXP	2	Jul			nde.	11253.216	-8591.2
E18	VSS	sinet				Þ	10338.816	-8591.2
E2	RSVD	der			18fille		19663.918	-9039.8
E20	PCIE7_RXP / SATA0_RXP	U.			unos		9424.416	-8591.2
E21	VSS			. se	3		8510.016	-8591.2
E22	PCIE9_RXN			Jefin			7595.616	-8591.2
E23	PCIE9_RXP			un			6681.216	-8591.2
E25	PCIE10_RXP		tine (du	5766.816	-8591.2
E27	PCIE11_RXP / SATA1B_RXP		undell			ndefine	4852.416	-8591.2
E28	PCIE11_RXN / SATA1B_RXN	cine			6	011.	3938.016	-8591.2
E3	RSVD	den			stine		19013.678	-9039.8
E30	PCIE12_RXN / SATA2_RXN	d un.			unde		3023.616	-8591.2
E32	VCC_SENSE			sine	,		2109.216	-8591.2
E33	VSS_SENSE			derr			1194.816	-8591.2
E35	XTAL24_OUT			JUN			280.416	-8591.2
E37	XTAL24_IN		sine			ed i	-633.984	-8591.2
E38	CLKOUT_PCIE_P5		nde.			18fille	-1548.384	-8591.2
E40	CLKOUT_PCIE_N5		du.			unos	-2462.784	-8591.2
E42	XCLK_BIASREF	Stille					-3377.184	-8591.2
E43	CLKOUT_ITPXDP_P	inde			defin.		-4291.584	-8591.2
E45	EDP_AUXN	<i>,d ,</i>			y une		-5205.984	-8591.2
E46	VSS			40	P ^{C4}		-6120.384	-8591.2
E48	DDI2_AUXN			dein			-7034.784	-8591.2
E5	PCIE_RCOMPP			d un			17654.016	-8591.2
E50	VSS		nia_	6		69	-7949.184	-8591.2
E52	eDP_RCOMP		nde.			~ efille	-8863.584	-8591.2
E53	VSS		0 V.			unu	-9777.984	-8591.2
E55	DDI1_TXN[0]	ii)				D.	-10692.384	-8591.2
E56	VSS	nor			detin		-11606.784	-8591.2
E58	DDI1_TXN[1]	ed ~		ned undefil	, un		-12521.184	-8591.2



B-Table 9-1. U/U-Quad Core Processor Ball List (Sheet 30 of 39)

	(intel)			under			define	
	Table 9-1. U/U-	Quad Core P	rocessor Ba	all List (She	et 30 of 39)	aned un		
Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- Interleaved (NIL)	X[um]	Y[um]
E6	VSS	deil.			enne		16739.616	-8591.29
E60	CFG_RCOMP	d vit			Inoc		-13435.584	-8591.29
E61	RSVD	Ì			Ò.		-14349.984	-8591.29
E63	CFG[16]			16111			-15315.184	-8654.79
E65	VSS			uno			-16331.184	-8654.79
E66	CFG[18]		in	0		- 20	-17347.184	-8654.79
E68	CFG[0]		dein			sines	-17898.618	-9363.45
E70	CFG[4]		1 UN			nde	-19664.172	-9009.12
E71	VSS	ei n ^e			d		-20314.412	-8901.17
E8	ITP_PMODE	der			i afino		15825.216	-8591.29
F1	VSS	d 01			Inor		19989.038	-8465.82
F10	USB3_4_RXP	5			eQ.		14910.816	-7941.05
F11	PCIE2_RXP / USB3_6_RXP			ndefin			13996.416	-7941.05
F13	VSS			du.			13082.016	-7941.05
F15	PCIE4_RXP		117			Loed	12167.616	-7941.05
F16	PCIE5_RXN		nde			Aeth.	11253.216	-7941.05
F18	PCIE6_RXP		9			UNU	10338.816	-7941.05
F2	VSS	efin			ine'	0	19338.798	-8465.8
F20	PCIE7_RXN / SATA0_RXN	dunas			Inden		9424.416	-7941.05
F21	PCIE8_RXP / SATA1A_RXP	6			ed		8510.016	-7941.05
F22	VSS			der			7595.616	-7941.05
F23	VSS			dun.			6681.216	-7941.05
F25	PCIE10_RXN		13.	net		d	5766.816	-7941.05
F27	VSS		nde.			18filte	4852.416	-7941.05
F28	VSS		du.			. unos	3938.016	-7941.05
F30	PCIE12_RXP / SATA2_RXP	defi			nia	0	3023.616	-7941.05
F32	VSS	d une			nde.		2109.216	-7941.05
F33	VSS	ner			ed v.		1194.816	-7941.05
F35	VSS			10	11-		280.416	-7941.05
F37	VSS			unor			-633.984	-7941.05
F38	VSS			ed -			-1548.384	-7941.05
F4	VSS		Je	11.		-tine	18363.438	-8465.8
F40	VSS		, un			der.	-2462.784	-7941.05
F42	VSS	đ	neo			d UN	-3377.184	-7941.05
F43	CLKOUT_ITPXDP_N	96	• *		113		-4291.584	-7941.05
F45	EDP_AUXP	, un-			nde.		-5205.984	-7941.05
F46	RSVD	inec			cined U.		-6120.384	-7941.05
	162			afined unde		Datasheet	, Volume 1 of 2	2
	una		Inde	37		defin		
						d une		



/YProcessor BallInformation U/U-Quad Core Processor Ball List (Sheet 31 of 39)

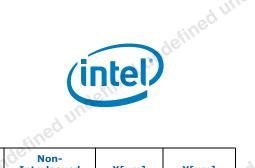
	ed unoc	essor BallInform		Indefilit		<u> </u>	ntel	
inde	Table 9-1. U/U-0	Quad Core P	rocessor Ba	ll List (Shee	et 31 of 39)	sined un		
Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- Interleaved (NIL)	X[um]	Y[um
F48	DDI2_AUXP	der			16tine		-7034.784	-7941.0
F5	PCIE_RCOMPN	0.1			inor		17654.016	-7941.0
F50	DDI1_AUXP			eo			-7949.184	-7941.0
F52	RSVD			Actin			-8863.584	-7941.0
F53	DDI1_TXN[2]			una		~	-9777.984	-7941.0
F55	DDI1_TXP[0]		ine ^o	-		d ut	-10692.384	-7941.0
F56	DDI1_TXN[3]		detti			sinet	-11606.784	-7941.0
F58	DDI1_TXP[1]	2	UNC			der.	-12521.184	-7941.0
F6	RSVD	sines			d 1		16739.616	-7941.0
F60	RSVD	deit			infine		-13435.584	-7941.0
F61	RSVD	UN.			inde		-14349.984	-7941.0
F63	CFG[17]						-15315.184	-8004.5
F65	VSS			etine			-16331.184	-8004.5
F66	CFG[19]			INOC			-17347.184	-8004.5
F68	VSS		e	A			-18561.812	-8320.0
F70	CFG[10]		16111			cineo.	-19212.052	-8320.0
F71	CFG[8]		una			"gerr.	-19862.292	-8383.5
F8	VSS				2	0.1.1	15825.216	-7941.0
G1	CL_RST#	Yeth.			sine		20314.158	-7802.
G10	VSS	, uno			nde'		14910.816	-7290.8
G11	PCIE2_RXN / USB3_6_RXN			eine	<i>d 1</i> .		13996.416	-7290.8
G13	PCIE1_RXP / USB3_5_RXP			under			13082.016	-7290.8
G15	PCIE4_RXN			0		24	12167.616	-7290.8
G16	PCIE3_RXP		4erin.			since	11253.216	-7290.8
G18	PCIE6_RXN		JUNG			der	10338.816	-7290.8
G2	CL_DATA	an ^e	,O		5-	U	19663.918	-7802.
G20	VCCSTG	gern.			sine		9424.416	-7290.8
G21	PCIE8_RXN / SATA1A_RXN	d une			4 unde		8510.016	-7290.8
G22	VSS			0	eo		7595.616	-7290.8
G23	VCCSA			dein			6681.216	-7290.8
G25	VCCSA			d un			5766.816	-7290.8
G27	VCCSA		7/2	2~		6	4852.416	-7290.8
G28	VCCSA		der			stine	3938.016	-7290.8
G3	CL_CLK		-d un			1000	19013.678	-7802.
G30	VCC	213-			~?	2	3023.616	-7290.8
G32	VCC	nder			16/11		2109.216	-7290.8
G33	VCC	dui		ned undefi	Inos		1194.816	-7290.8

(intel) ed undefine

U/U-Quad Core/YProcessor BallInformation

B-Table 9-1. U/U-Quad Core Processor Ball List (Sheet 32 of 39)

nu s	Table 9-1. U/U-C	Quad Core P	rocessor Ba	all List (She	et 32 of 39)	1 stines		[
O Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- Interleaved (NIL)	X[um]	Y[um]
G35	VCC	nder			18fin		280.416	-7290.83
G37	VCC) US			unos		-633.984	-7290.83
G38	VCC				<u>,</u>		-1548.384	-7290.8:
G4	GPP_E2 / SATAXPCIE2 / SATAGP2			defin			18363.438	-7802.8
G40	VCC			0.00			-2462.784	-7290.83
G42	VCC		- fine			e o	-3377.184	-7290.8
G43	VSS		nòci			16/11	-4291.584	-7290.83
G45	VSS	0	9.7.			uno	-5205.984	-7290.83
G46	RSVD	e fine			e ⁰		-6120.384	-7290.83
G48	VSS	inde			dei		-7034.784	-7290.8
G5	VSS	Ò.			4 Une		17654.016	-7290.8
G50	DDI1_AUXN	·		275	(9 ⁰		-7949.184	-7290.8:
G52	VSS			gein.			-8863.584	-7290.8
G53	DDI1_TXP[2]			2 UN			-9777.984	-7290.8
G55	VSS		2/2	C.C.		6	-10692.384	-7290.8
G56	DDI1_TXP[3]		dell'			i chine	-11606.784	-7290.83
G58	VSS		- d uli			inde	-12521.184	-7290.83
G6	VSS	7173	20			<u>, , , , , , , , , , , , , , , , , , , </u>	16739.616	-7290.8
G60	VSS	nde''			1 etine		-13435.584	-7290.8
G61	VCC_OPC_1P8	-0. //··			Inos		-14349.984	-7290.8
G63	VSS	6-			ed v		-15315.184	-7354.3
G65	VSS			19			-16331.184	-7354.3
G66	VSS			Uno			-17347.184	-7354.3
G68	CFG[11]			eo.		6	-18363.692	
G69	CFG[9]		Jet!			· 3.01	-19013.932	-7659.62
G70			i uno.			-961.	-19664.172	-7758.68
	CFG[15] CFG[13]		eo.			.0. 		
G71 G8	USB3_1_RXP	dell	b		nin-		-20314.412 15825.216	-7758.68
	GPP_E8 / SATALED#	June			uger.			
H1 H10	USB3_3_RXP	?			60 V.		19989.038 14910.816	-7139.9 -6640.5
H10	RSVD	•		76			13996.416	-6640.5
H11 H13	PCIE1_RXN / USB3_5_RXN			d unos			13996.416	-6640.57
H15	VSS			Ne~		.0	12167.616	-6640.57
H15	PCIE3_RXN					i etine	12167.616	-6640.5
H18	VSS		red MI.			, una-	10338.816	-6640.5
H2	GPP E0 / SATAXPCIE0 /	.el	ne			ed	19338.798	-7139.9
	SATAGPO	1 unos			deth			
H20	VCCSA_SENSE	INEO			eo un		9424.416	-6640.5
	164			stined unde				len
	164			duns		Datasheet	, Volume 1 of 2	2
	10Th							



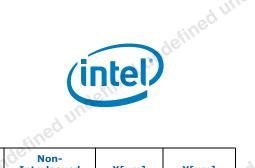
/YProcessor BallInformation U/U-Quad Core Processor Ball List (Sheet 33 of 39)

	od unou	essor BallInform		Indefine		C	ntel	
inde	Table 9-1. U/U-0	Quad Core P	rocessor Ba	II List (Shee	et 33 of 39)	tined une		
Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- Interleaved (NIL)	X[um]	Y[um]
H21	VSSSA_SENSE	ndell			16fine		8510.016	-6640.5
H3	GPP_E1 / SATAXPCIE1 / SATAGP1	0.			uno		18688.558	-7139.9
Н5	GPP_D19 / DMIC_CLK0			Concella international interna	~		17654.016	-6640.5
H6	USB3 2 RXP /			detil			16739.616	-6640.5
	SSIC_RXP		6-	UI.		10		
H63	VCC_OPC_1P8		tines			ed v	-15315.184	-6704.0
H65	OPC_RCOMP		de.			Jeff II	-16331.184	-6704.0
H66	OPCE_RCOMP	6	Q.			no	-17347.184	-6704.0
H69	CFG[14]	A HING			ine ⁰		-18688.812	-7095.74
H70	CFG[12] VSS	una			dein		-19339.052	-7095.7
H71	USB3_1_RXN			2	un		-19989.292 15825.216	-7095.7
H8 J1	GPP_E4 / DEVSLP0			FILLEL	1		20314.158	-6640.5 -6477
J1 J10	USB3_3_RXN						14910.816	-5990.3
J10 J11	VSS			<i>.</i>		i.	13996.416	-5990.3
J13	VSS		atine			red	13990.410	-5990.3
J15 J2	GPP_E5 / DEVSLP1		inde			Ye.	19663.918	-6477
J22	VCCSA	0			2	ano.	7138.416	-6826.5
J23	VCCSA	1911			^O 9 _{01i}		6224.016	-6826.5
J25	VSS	UNO			delli		5309.616	-6826.5
J27	VCCSA	ð -			d un		4395.216	-6826.5
J28	VSS			fine			3480.816	-6826.5
J3	GPP_E6 / DEVSLP2			.nder			19013.678	-6477
J30	VCC		0	0, 7,			2566.416	-6826.5
J32	VSS		enne	r		the o	1652.016	-6826.5
J33	VCC		inde			det	737.616	-6826.5
J35	VSS		ġ,		2	UNC	-176.784	-6826.5
J37	VCC	Jetit			sinet		-1091.184	-6826.5
J38	VSS	1 100			ndeit		-2005.584	-6826.5
]4	GPP_D3 / SPI1_MOSI	80			,d ^{VII}		18363.438	-6477
J40	VCC			nije			-2919.984	-6826.5
J42	VSS			inde			-3834.384	-6826.5
J43	VCCGT			20 V		2	-4748.784	-6826.5
J45	VCCGT		16fin			cin ^{co}	-5663.184	-6826.5
J46	VCCGT		uno			dem	-6577.584	-6826.5
J48	VCCGT		eo			Jul.	-7491.984	-6826.5
J5	GPP_D23 / I2S_MCLK	Yern			sine		17654.016	-5990.3
J50	VCCGT	1 UNS		ned undefil	der		-8406.384	-6826.5



B-Table 9-1. U/U-Quad Core Processor Ball List (Sheet 34 of 39)

	sineo			JUI!		١٢, ١٢	100	
nu.	Table 9-1. U/U-	Quad Core P	rocessor Ba	all List (She	et 34 of 39)	tined -	1	1
Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- Interleaved (NIL)	X[um]	Y[um]
J52	VCCGT	deil			enne		-9320.784	-6826.50
J53	VCCGT	N ON I			Inoc		-10235.184	-6826.50
J55	VCCGT				jo –		-11149.584	-6826.50
J56	VCCGT			16/11			-12063.984	-6826.50
J58	VCCGT			una			-12978.384	-6826.50
J6	USB3_2_RXN / SSIC_RXN		efine	,		ined u	16739.616	-5990.33
J60	VCCGT		inoc			den	-13892.784	-6826.50
J68	RSVD	~	9.2			Une	-18361.914	-6519.92
J69	VSSGT_SENSE	76 ₁₁₁ ,			sineo		-19013.932	-6432.80
J70	VCCGT_SENSE	. uno-			dette		-19664.172	-6432.80
J71	RSVD	0			2 Un		-20314.412	-6432.80
J8	VSS			272	(a)		15825.216	-5990.33
K15	VCCAMPHYPLL_1P0			"ger			12188.19	-5876.2
K16	VSS			duit			11537.95	-5876.2
K17	VCCMPHYAON_1P0		713	6		ed	10887.71	-5876.2
K18	VSS		nder.			16/11/2	10237.47	-5876.2
К19	VCCCLK2		9.7			unos	9587.23	-5876.2
K20	VccPLL	All A	6-		9	0.	8936.99	-5876.2
K21	VccPLL	nde			Actin		8286.75	-5876.2
K22	VSS	0.0			, unc		7595.616	-6361.68
K23	VCCSA	<u> </u>			deo.		6681.216	-6361.68
K25	VCCSA			den			5766.816	-6361.68
K27	VCCSA			4 UN			4852.416	-6361.68
K28	VCCSA		ć.	den.		6	3938.016	-6361.68
K30	VCCSA		ndell			- Alle	3023.616	-6361.68
K32	RSVD		duin			nde	2109.216	-6361.68
К33	VCC	13-	NG C.		-	0	1194.816	-6361.68
K35	VCC	nder			16th		280.416	-6361.68
K37	VCC	du			uno		-633.984	-6361.68
K38	vcc				heo		-1548.384	-6361.68
K40	VCC			Je.			-2462.784	-6361.68
K42	VCC			1 Unic			-3377.184	-6361.68
K43	VCC		e e	neu			-4291.584	-6361.68
K45	RSVD		de			Aine	-5205.984	-6361.68
K46	RSVD		dune			inde.	-6120.384	-6361.68
K48	VCCGT	ć	nor			0.0	-7034.784	-6361.68
K50	VCCGT	~de)	~		1891	~	-7949.184	-6361.68
K52	VCCGT	-d ull'					-8863.584	-6361.68
	40	ine	I		fined t.	1		ed une
	166			stined unde	9°	Datasheet	, Volume 1 of 2	2
	ndefine			fineo			sq n.	
	UI.		ndk			76tII.		



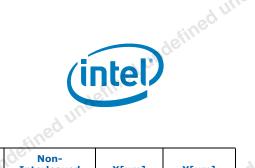
/YProcessor BallInformation U/U-Quad Core Processor Ball List (Sheet 35 of 39)

Table 9-1. U/U-C Ball Name	Quad Core P	rocessor Ba	II List (Shee DDR4	t 35 of 39) Interleaved (IL)	Non- Interleaved (NIL)	X[um] -9777.984 -10692.384	Y[um -6361.6
/CCGT /CCGT /CCGT /CCGT /CCGT	DDR3L	LPDDR3	DDR4		Interleaved	-9777.984	-6361.6
rccgt rccgt rccgt rccgt rccgt	uder.		OS CONTRACTOR	undefine			<u> </u>
YCCGT YCCGT YCCGT			090	uno		-10692.384	
/CCGT /CCGT			eo.				-6361.6
/CCGT						-11606.784	-6361.6
			Activ			-12521.184	-6361.6
SS	1		Une			-13435.584	-6361.6
		ine ^o	-		dutt	-14349.984	-6361.6
'SS		detti			Aines	-15132.812	-6054.0
'SS	2	Une			nde'	-15783.052	-6054.0
'SS	eineo			, d t		-16433.292	-6054.0
'SS	der			fine		-17083.532	-6054.0
'SS	V			. nor		-17733.772	-6054.0
'SS			e.C			-18351.754	-5846.0
'SS			1.efin.s			-19339.052	-5744.4
'SS			inde			-19989.292	-5744.4
CCMPHYAON_1P0		e				19989.038	-5814.0
GPP_E17 / EDP_HPD		76/11/2			cin ^{eo}		-5340.0
'SS		uno			der		-5340.0
GPP_E19 / DDPB_CTRLDATA	Lefiner			ined	0111	13683.996	-5340.0
GPP_E18 / DDPB_CTRLCLK	Junoc			inden		13033.756	-5340.0
CCAMPHYPLL_1P0			- 2	9. 0.		12188.19	-5038.0
'SS			1efille			11537.95	-5038.
'SS			, unos			10887.71	-5038.
'SS			Ò,		20	10237.47	-5038.
CCCLK5		46th.			sine	9587.23	-5038.
'SS		, une			der	19338.798	-5814.
'SS		,o		6	UL.	8936.99	-5038.
CCCLK3	dern.			sine		8286.75	-5038.
'SS	1 1112			der		18363.438	-5814.
GPP_E15 / DDPD_HPD2	800			00		17585.436	-5340.0
CCGT			nije			-14643.862	-5624.
CCGT			inde.			-15112.492	-5167.0
CCGT			<u>,</u> d			-15762.732	-5167.
CCGT		Aefin			^O SN:5	-16412.972	-5167.
CCGT		Inde			dein	-17063.212	-5167.
		A V			Un	-17713.452	-5167.
CCGT		ev					
	10 ^{fir}	eu		Sine sine	0	-18363.692	-5167.
	SS SS SS SS SS SS SS SS SS SS SS SS SS	SS	SS SS SS SS SS SS SS SS SS SS SS SS CCMPHYAON_1P0 SS PP_E17 / EDP_HPD SS SS SS IPP_E19 / SS IPP_E18 / SS IPP_E18 / SS SS SS	SS	SS Image: SS <	SSImage: ssign set in the state	SS Image: SS <thimage: ss<="" th=""> <thimage:< th=""></thimage:<></thimage:>



ed undefined undefined Table 9-1. U/U-Quad Core Processor Ball List (Sheet 36 of 39)

	(intel)			defins	07 0-Quau C0	ore/YProcessor Ba		•
				Un			Ige.	
	Table 9-1. U/U-Q)uad Core P	rocessor Ba	» III List (She	et 36 of 39)	ed u		
Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- Interleaved (NIL)	X[um]	Y[um]
L7	GPP_E14 / DDPC_HPD1	detin			i stinet	()	16935.196	-5340.09
L70	VCCGT	U.			. inde		-19664.172	-5167.63
L71	VCCGT	r		- 9	b		-20314.412	-5167.63
L8	VSS			1efine			16284.956	-5340.09
L9	GPP_E13 / DDPB_HPD0			inoc			15634.716	-5340.09
M1	GPP_D0 / SPI1_CS#			<u>P</u>		20	20314.158	-5151.12
M2	GPP_D1 / SPI1_CLK		Yeth			.ineu	19663.918	-5151.12
M3	GPP_D2 / SPI1_MISO		UNU			JOC/	19013.678	-5151.12
M4	GPP_D5 / ISH_I2C0_SDA	etine	0		ined	01.	18363.438	-5151.12
M62	VCCGT	ince			dert		-14643.862	-4710.43
N1	GPP_D7 / ISH_I2C1_SDA	0			ed une		19989.038	-4488.18
N10	VSS			ACTIN			14984.476	-4400.29
N11	GPP_E22			, unc.			14334.236	-4400.29
N12	GPP_E23			eo.		6	13683.996	-4400.29
N13	VSS		dein.			sines	13033.756	-4400.29
N15	VCCMPHYGT_1P0		4 UNC			nde.	12188.19	-4199.89
N16	VCCMPHYGT_1P0	γ_{i5}	S			8 01.	11537.95	-4199.89
N17	VCCMPHYGT_1P0	der			AINE		10887.71	-4199.89
N18	VCCAPLLEBB_1P0	2 Un			inde		10237.47	-4199.89
N19	VSS	8 -			ed V		9587.23	-4199.8
N2	GPP_D8 / ISH_I2C1_SCL			illes i			19338.798	-4488.1
N20	VCCCLK4			INOS			8936.99	-4199.8
N21	VSS			ed		2	8286.75	-4199.8
N3	GPP_D6 / ISH_I2C0_SCL		16/11			ein ^{ec}	18688.558	-4488.1
N6	VSS		. uno-			der	17585.436	-4400.29
N63	VCCGT		ed t			d un	-15112.492	-4253.2
N64	VCCGT	yeii			nia.	3	-15762.732	-4253.2
N65	VSS	1 UNU			der		-16412.972	-4253.2
N66	VCCGT	100			~d v''		-17063.212	-4253.2
N67	VCCGT	•		2	NG-		-17713.452	-4253.2
N68	VSS			nde			-18363.692	-4253.2
N69	VCCGT			ed vi			-19013.932	-4253.2
N7	GPP_E20 / DDPC_CTRLCLK		def	NU.		efine	16935.196	-4400.29
N70	VCCGT		dui			Inoc	-19664.172	-4253.2
N71	VCCGT		ne			ed	-20314.412	-4253.2
N8	GPP_E21 / DDPC_CTRLDATA	unde			odefil		16284.956	-4400.29
N9	GPP_E16 / DDPE_HPD3	neo			-d un		15634.716	-4400.29
	der				fine			ed
	168 undefined undef			tined unde		Datasheet	t, Volume 1 of 2	2
	June		, unde			adefin		
sino			- CO			d UIT.		



/YProcessor BallInformation U/U-Quad Core Processor Ball List (Sheet 37 of 39)

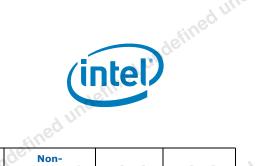
Ball Name 12 PHYGT_1P0 PHYGT_1P0 IM_1P0 9 10 11 PC 2 / SMBALERT# KLTCTL	Quad Core P	rocessor Ba	II List (Shee	t 37 of 39)	Non- Interleaved (NIL)	X[um] 20314.158 12188.19 11537.95 10887.71 10237.47 9587.23	Y[um] -3825.2 -3361.6 -3361.6 -3361.6
12 PHYGT_1P0 PHYGT_1P0 IM_1P0 9 10 11 12 2 / SMBALERT#	DDR3L	LPDDR3	DDR4		Interleaved	20314.158 12188.19 11537.95 10887.71 10237.47 9587.23	-3825.2 -3361.6 -3361.6 -3361.6 -3361.6
PHYGT_1P0 PHYGT_1P0 IM_1P0 9 10 11 11 PC 2 / SMBALERT#	under .	undefined	undefined		eined un	12188.19 11537.95 10887.71 10237.47 9587.23	-3361.6 -3361.6 -3361.6 -3361.6
PHYGT_1P0 IM_1P0 9 10 11 12 2 / SMBALERT#	underined	undefined	undefined	JULO	eined un	11537.95 10887.71 10237.47 9587.23	-3361.6 -3361.6 -3361.6
IM_1P0 9 10 11 2 / SMBALERT#	underined	undefined	undefineo		eined un	10887.71 10237.47 9587.23	-3361.6 -3361.6
9 10 11 2 / SMBALERT#	underined	undefined	unden		inu banis	10237.47 9587.23	-3361.6
9 10 11 2 / SMBALERT#	underined	undefined	nue		ined un	9587.23	
10 11 2 / SMBALERT#	undefined	undefinec			cined ut		
10 11 2 / SMBALERT#	undefined	under			nin -	1 1	-3361.
11 PC 2 / SMBALERT#	undefined	UL				19663.918	-3825.2
11 PC 2 / SMBALERT#	undefiner				000	8936.99	-3361.0
11 PC 2 / SMBALERT#	under			ed v		8286.75	-3361.6
2 / SMBALERT#				1 stine		19013.678	-3825.2
2 / SMBALERT#		1		INOS		18363.438	-3825.2
			ec			-14643.862	-3796.0
KLTCTL			return			14984.476	-3333.4
			uno			14334.236	-3333.4
KLTEN		100	>		dui	13683.996	-3333.4
		Yeun			sines	13033.756	-3333.4
		Unv			der	17585.436	-3333.4
-	ine	>		6-		-15112.492	-3338.
-	deitt			Since		-15762.732	-3338.
-	A UNC			ndei		-16412.972	-3338.
sine	0		0	<i>b'</i> ''		-17063.212	-3338.8
der			- fine			-17713.452	-3338.8
dull			inde			-18363.692	-3338.
NGC.		- 2	Ò		_ V	-19013.932	-3338.8
0 / SMBCLK		18tin			OSn:	16935.196	-3333.4
		. unos			deili		-3338.
-		iq .		2	UN		-3338.
1 / SMBDATA	76111			sineu	¢		-3333.4
	1 UNC			de'			-3333.4
	20 20			0.01		19989.038	-3162
-9erin			nia.	e -			-2523.
PPE			inde.			11537.95	-2523.
Ner.			<u>, d '''</u>			10887.71	-2523.
*		nije,			red	-	-2523.
AM_1P0		Inde			Jenn.	9587.23	-2523.4
		ed			JUNY	19338.798	-3162
AM_1P0	1011	~		Shin	<u>0</u>		-2523.4
	, unor			-9e.I.			-2523.
			- - - - - - - <td< th=""><th>Image: Constraint of the second se</th><th>Image: system of the system</th><th>Image: Second second</th><th>Image: Sector of the sector</th></td<>	Image: Constraint of the second se	Image: system of the system	Image: Second	Image: Sector of the sector





ed undefined undefined Table 9-1. U/U-Quad Core Processor Ball List (Sheet 38 of 39)

in ^k	Table 9-1. U/U-0	Quad Core P	rocessor Ba	all List (She	et 38 of 39)	fined L		
Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- Interleaved (NIL)	X[um]	Y[um]
T4	VSS	deil			erine		18363.438	-3162.
T62	VCCGT	, Ut			unor		-14643.862	-2881.6
U1	GPP_D13 / ISH_UART0_RXD / SML0BDATA / I2C4B_SDA			undefine	0		20314.158	-2499.3
U10	VSS		-9	0		_ U	14984.476	-2266.69
U11	RSVD		16/11/2			sineu	14334.236	-2266.6
U12	RSVD		inos			gerr	13683.996	-2266.6
U13	eDP_VDDEN		0		6	UL	13033.756	-2266.6
U2	GPP_D14 / ISH_UART0_TXD / SML0BCLK / I2C4B_SCL	4 undefin.			ndefinec		19663.918	-2499.3
U3	GPP_D15 / ISH_UART0_RTS#				d ^U		19013.678	-2499.3
U4	GPP_D16 / ISH_UART0_CTS# / SML0BALERT#			undefin			18363.438	-2499.3
U6	GPP_C17 / I2C0_SCL			ed.		6	17585.436	-2266.6
U63	VSS		Yelli	*		sinet.	-15112.492	-2424.4
U64	VSS		1 Unit			del	-15762.732	-2424.4
U65	VCCGT	20	20			8.00	-16412.972	-2424.4
U66	VSS	defi			sine		-17063.212	-2424.4
U67	VSS	2 UN			nde.		-17713.452	-2424.4
U68	VCCGT	0			d'u		-18363.692	-2424.4
U69	VSS			il.			-19013.932	-2424.4
U7	GPP_C16 / 12C0_SDA			Inde			16935.196	-2266.6
U70	VSS			100 V		2	-19664.172	-2424.4
U71	VCCGT		196			cineo	-20314.412	-2424.4
U8	GPP_C18 / I2C1_SDA		, uno-			der	16284.956	-2266.6
U9	GPP_C19 / I2C1_SCL		ec			dull	15634.716	-2266.6
V1	GPP_D21 / SPI1_IO2	dett	. *		nij-		19989.038	-1836.4
V15	VCCAPLL_1P0	JUNG			nde.		12188.19	-1685.2
V16	VSS	neu			ed u.		11537.95	-1685.2
V17	VSS		1		Nr.		10887.71	-1685.2
V18	VSS			, inde			10237.47	-1685.2
V19	VCCPRIM_3p3			Leo L			9587.23	-1685.2
V2	GPP_D22 / SPI1_IO3		16			sine	19338.798	-1836.4
V20	VCCPRIM_CORE		, unos			dett	8936.99	-1685.2
V21	VCCPRIM_CORE		neo			duit	8286.75	-1685.2
V3	GPP_C7 / SML1DATA	Ye			113	0	18688.558	-1836.4
V62	VCCOPC	, un			nder.		-14643.862	-1967.2
	170	IUGE		stined unde	stined L	Datasheet	, Volume 1 of 2	led un



/YProcessor BallInformation U/U-Quad Core Processor Ball List (Sheet 39 of 39) Table 9-1.

W11 GPP_G4 / SD_DATA3 Image: Mail of the mail		0/0-Quad Core/ TProce			Indefili		C	ntel	
Ball Name DDR3L LPDDR3 DDR4 Litterated (TL) Interleaved (TL) X[um] W1 GPP_C5 / SML0ALERT# 20314.158 20314.158 W10 GPP_G5 / SD_CD# 14984.476 14984.476 W11 GPP_G4 / SD_DATA3 14334.236 W12 GPP_G3 / SD_DATA2 13683.996 13033.756 W13 VSS 19013.678 19013.678 W3 GPP_C4 / SMLDATA 19013.678 19013.678 W4 GPP_C1 / UARTO_RTS# 1933.763 1933.763 W4 GPP_C1 / UARTO_RTS# 1933.678 1933.763 W63 VCCGT 17585.436 1935.436 W63 VCCGT 1512.492 16412.972 W64 VCCGT 16139.333 1633.33	nde	Table 9-1. U/U-0	Quad Core P	rocessor Ba	ll List (Shee	et 39 of 39)	sined un		
W10 GPP_G5 / SD_CD# Image: Constraint of the second secon	Ball #	Bali Name	DDR3L	LPDDR3	DDR4		Interleaved	X[um]	Y[um]
W11 GPP_G4 / SD_DATA3 Image: constraint of the system 14334.236 14334.236 W12 GPP_G3 / SD_DATA2 Image: constraint of the system 13033.756 13033.756 W2 GPP_C4 / SML0DATA Image: constraint of the system 1963.918 13033.756 W2 GPP_C6 / SML1CLK Image: constraint of the system 19013.678 19013.678 W4 GPP_C10 / UARTO_RTS# Image: constraint of the system 18363.438 17585.436 W6 VSS Image: constraint of the system Image: constraint of the system 17585.436 W64 VCCGT Image: constraint of the system Image: constraint of the system 15112.492 W64 VCCGT Image: constraint of the system Image: constraint of the system 15112.492 W64 VCCGT Image: constraint of the system Image: constraint of the system 15112.492 W64 VCCGT Image: constraint of the system Image: constraint of the system 16412.972 W66 VCCGT Image: constraint of the system Image: constraint of the system 17063.212 W67	W1	GPP_C5 / SML0ALERT#	nder			164100		20314.158	-1173.4
W12 GPP_G3 / SD_DATA2 13683.996 W13 VSS 13033.756 W2 GPP_C4 / SMLODATA 1963.918 W3 GPP_C6 / SML1CLK 19013.678 W4 GPP_C10 / UARTO_RTS# 18363.438 W6 VSS 17585.436 W63 VCCGT 15112.492 W64 VCCGT 15112.492 W65 VCCGT 15112.492 W64 VCCGT 15112.492 W65 VCCGT 15112.492 W66 VCCGT 1562.732 W66 VCCGT 17713.452 W67 VCCGT 17713.452 W68 VCCGT 16935.196 W70 VCCGT 16935.196 W71 VCCGT 16935.196 W71 VCCGT 16284.956 W9 VSS 16284.956 W9 VSS 16284.956 W9 VSS 16284.956 W9 VSS 16284.956 W9	W10	GPP_G5 / SD_CD#	0.			uno		14984.476	-1199.89
W13 VSS 13033.756 W2 GPP_C4 / SMLODATA 19663.918 W3 GPP_C6 / SMLICLK 19013.678 W4 GPP_C10 / UARTO_RTS# 18363.438 W6 VSS 17585.436 W63 VCCGT 17585.436 W64 VCCGT 15112.492 W64 VCCGT 16112.492 W65 VCCGT 1711.452 W66 VCCGT 1711.452 W67 VCCGT 1711.452 W68 VCCGT 18363.692 W69 VCCGT 16935.196 W70 VCCGT 16935.196 W71 VCCGT 16935.196 W71 VCCGT 16935.196 W71 VCCGT 16284.956 W9	W11	GPP_G4 / SD_DATA3			eo			14334.236	-1199.89
W2 GPP_C4 / SMLODATA 19663.918 W3 GPP_C6 / SML1CLK 19013.678 W4 GPP_C10 / UART0_RTS# 18363.438 W6 VSS 17585.436 W63 VCCGT 15112.492 W64 VCCGT 15172.492 W64 VCCGT 15172.492 W64 VCCGT 16412.972 W65 VCCGT 17685.212 W67 VCCGT 1713.452 W68 VCCGT 18363.692 W69 VCCGT 16935.196 W70 VCCGT 16935.196 W70 VCCGT 16935.196 W71 VCCGT 16935.196 W71 VCCGT 16935.196 W71 VCCGT 16284.956 W9 VSS 16284.956 W9 11537.9	W12	GPP_G3 / SD_DATA2			Activ			13683.996	-1199.89
W3 GPP_C6 / SML1CLK Image: Constraint of the system of th	W13	VSS			Une		0	13033.756	-1199.89
W4 GPP_C10 / UART0_RTS# Image: Constraint of the system o	W2	GPP_C4 / SML0DATA		ineo			-d vii	19663.918	-1173.4
W6 VSS Intervention Intervention <thintervention< th=""> <thintervention< th=""> Inte</thintervention<></thintervention<>	W3	GPP_C6 / SML1CLK		detit			sines	19013.678	-1173.4
W63 VCCGT -15112.492 W64 VCCGT -15762.732 W65 VCCGT -16412.972 W66 VCCGT -16412.972 W67 VCCGT -17063.212 W67 VCCGT -17063.212 W68 VCCGT -1701.452 W69 VCCGT -1701.3452 W69 VCCGT -1901.3932 W7 GPP_G7 / SD_WP -1901.3932 W7 GPP_G7 / SD_WP -1901.3932 W71 VCCGT -1901.412 W8 GPP_G6 / SD_CLK -19064.172 W71 VCCGT -20314.412 W8 GPP_G6 / SD_CLK -16284.956 W9 VSS 15634.716 Y15 VCCGPPD -112188.19 Y16 VCCPGPPC 10237.47 Y18 VCCPRIM_1p0 10237.47 Y19 VSS 9587.23 Y20 VSS -10 8936.99	W4	GPP_C10 / UART0_RTS#	2	Un			nde.	18363.438	-1173.4
W64 VCCGT -15762.732 W65 VCCGT -16412.972 W66 VCCGT -17063.212 W67 VCCGT -17713.452 W68 VCCGT -17713.452 W68 VCCGT -19013.932 W7 GPP_G7 / SD_WP -19013.932 W7 GPP_G7 / SD_WP -19064.172 W71 VCCGT -19064.172 W71 VCCGT -19064.172 W71 VCCGT -15634.716 W71 VCCGT -15634.716 W71 VCCGT -15634.716 W71 VCCGT -15634.716 W71 VCCGT -11713.452 W8 GPP_G6 / SD_CLK -19664.172 W71 VCCGT -19664.172 W71 VCCGT -116284.956 W9 VSS 15634.716 Y15 VCCPGPPD 11537.95 Y16 VCCPGPPC 11837.95 Y17 VSS 10887.71 Y	W6	VSS	sineu			6		17585.436	-1199.89
W65 VCCGT -16412.972 W66 VCCGT -17063.212 W67 VCCGT -17713.452 W68 VCCGT -1713.452 W68 VCCGT -19113.932 W7 GPP_G7 / SD_WP -19013.932 W7 GPP_G7 / SD_WP -19641.172 W71 VCCGT -19664.172 W71 VCCGT -19664.172 W71 VCCGT -20314.412 W8 GPP_G6 / SD_CLK -20314.412 W8 GPP_G6 / SD_CLK -15634.716 Y15 VCCPGPPD -11537.95 Y16 VCCPGPPC -111537.95 Y17 VSS -10887.71 Y18 VCCPRIM_1p0 -10111111 Y19 VSS -1011111 Y19 VSS -101111 Y20 VSS -10111	W63	VCCGT	der			interine		-15112.492	-1510.0
W66 VCCGT Image: Construct of the second se	W64	VCCGT	0			. more	1	-15762.732	-1510.0
W67 VCCGT -17713.452 W68 VCCGT -18363.692 W69 VCCGT -19013.932 W7 GPP_G7 / SD_WP -1903.932 W70 VCCGT 16935.196 W70 VCCGT -19064.172 W71 VCCGT -20314.412 W8 GPP_G6 / SD_CLK -20314.412 W8 GPP_G6 / SD_CLK 16284.956 W9 VSS 15634.716 Y15 VCCGPPD 111337.95 Y17 VSS 10887.71 Y18 VCCPRIM_1p0 10237.47 Y19 VSS 9587.23 Y20 VSS 8936.99	W65	VCCGT			e.C		1	-16412.972	-1510.0
W68 VCCGT	W66	VCCGT			18fine			-17063.212	-1510.0
NGC CCGT COUNCIDE W69 VCCGT -19013.932 W7 GPP_G7 / SD_WP 16935.196 W70 VCCGT -19664.172 W71 VCCGT -19664.172 W71 VCCGT -20314.412 W8 GPP_G6 / SD_CLK 16284.956 W9 VSS 15634.716 Y15 VCCPGPPD 12188.19 Y16 VCCPGPPC 11537.95 Y17 VSS 10887.71 Y18 VCCPRIM_1p0 10237.47 Y19 VSS 9587.23 Y20 VSS 8936.99	W67	VCCGT			INO			-17713.452	-1510.0
W7 GPP_G7 / SD_WP Image: Constraint of the system Image: Cons	W68	VCCGT		e	A		A U	-18363.692	-1510.0
W70 VCCGT -19664.172 W71 VCCGT -20314.412 W8 GPP_G6 / SD_CLK 16284.956 W9 VSS 15634.716 Y15 VCCPGPPD 12188.19 Y16 VCCPGPPC 11537.95 Y17 VSS 10887.71 Y18 VCCPRIM_1p0 10237.47 Y19 VSS 9587.23 Y20 VSS 8936.99	W69	VCCGT		10till			cineu	-19013.932	-1510.0
W71 VCCGT	W7	GPP_G7 / SD_WP		una			deili	16935.196	-1199.89
W71 VCCGT -20314.412 W8 GPP_G6 / SD_CLK 16284.956 16284.956 W9 VSS 15634.716 15634.716 Y15 VCCPGPPD 12188.19 12188.19 Y16 VCCPGPPC 11537.95 11537.95 Y17 VSS 10887.71 10887.71 Y18 VCCPRIM_1p0 1011111 10237.47 Y19 VSS 1011111 9587.23 Y20 VSS 1011111 8936.99	W70	VCCGT		÷		6	O/	-19664.172	-1510.0
W8 GPP_G6 / SD_CLK 16284.956 W9 VSS 15634.716 Y15 VCCPGPPD 12188.19 Y16 VCCPGPPC 11537.95 Y17 VSS 10887.71 Y18 VCCPRIM_1p0 10237.47 Y19 VSS 9587.23 Y20 VSS 10	W71	VCCGT	AC, III			AIL CO			-1510.0
W9 VSS 15634.716 Y15 VCCPGPPD 12188.19 Y16 VCCPGPPC 11537.95 Y17 VSS 10887.71 Y18 VCCPRIM_1p0 10237.47 Y19 VSS 9587.23 Y20 VSS 8936.99	W8	GPP_G6 / SD_CLK	1 Uno			nde'.			-1199.89
Y15 VCCPGPPD 12188.19 Y16 VCCPGPPC 11537.95 Y17 VSS 10887.71 Y18 VCCPRIM_1p0 10237.47 Y19 VSS 9587.23 Y20 VSS 9936.99	W9	0	D.			<i>3</i>			-1199.89
Y17 VSS 10887.71 Y18 VCCPRIM_1p0 10237.47 Y19 VSS 9587.23 Y20 VSS 8936.99	Y15	VCCPGPPD			ALL STREET				-847.09
Y17 VSS 10887.71 Y18 VCCPRIM_1p0 10237.47 Y19 VSS 9587.23 Y20 VSS 8936.99	Y16	VCCPGPPC			nde			11537.95	-847.0
Y18 VCCPRIM_1p0 10237.47 Y19 VSS 9587.23 Y20 VSS 8936.99		CV.		.0	Ò.				-847.0
Y19 VSS 9587.23 Y20 VSS 8936.99	·	VCCPRIM 1p0		i atin'	r		ineo i		-847.0
Y20 VSS 8936.99		*		inde			dein.	_	-847.0
Y21 VSS 8286.75 Y62 VCCGT -14643.862	Y20	VSS		0.		2	UNC		-847.0
VCCGT -14643.862 Datasheet, Volume 1 of 2 171	Y21	VSS	76/11			sinel			
Datasheet, Volume 1 of 2 171	Y62	VCCGT	, uno-			dell.		-14643.862	-1052.8
Datasheet, Volume 1 of 2		d undefin	0		ndefin	ed ut		definer	Junde
Datasheet, Volume 1 of 2	tined "	Indefinec		ed undefin	edu		undefined	unc	
Datasheet, Volume 1 of 2			red undefin			d undefine			inde
nder. define		Datasheet, Volume 1 of 2			ed undefil			undefine 171	ġ.
indelling aunor		under		d undefil	ne .		indefined		

(intel) red under

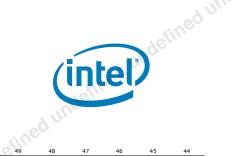
9.2

ndefined und

ed undefined undefined **Y-Processor Ball Information**

Jeffined unde A magined underned un

12 manual undermed undermed

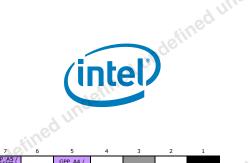


	<u>ا</u> ں <u>د</u>	64	63	62	61	60	59 59	58	I Map 57	(Up) 56	55 per Lo	eft, C 54	olum	ns 64 52	-44)	50	49	48	47	46	45	44	
1efin	BP VI BN VI	DDQ DDQ		DDR0_BA[0]7 DDR0_CAB [4]/ DDR0_BA[DDR0_ODT [0]			VDDQ DDR0_MA[1]7 DDR0_CAB	Ø.	VDDQ	DDR1_DQ[20] / DDR0_DQ[52]		DDR1_DQ[21] / DDR0_DQ[53]		DDR1_DQ[29] / DDR0_DQ[61]	VDDQ	DDR1_DQ 28] / DDR0_DQ 60]		DDR_VTT_ CNTL		DDR0_DQ[48] / DDR1_DQ[32]	r r	unde
nos	вм			DDRO <u>B</u> A[0]			DDR0_MA[10]/ DDR0_CAB	[8]/ DDR0_MA[1]		DDR0_PAR	52]	DDR1_DQ9 N[2] /	53]	DDR1_DQ[22]/ DDR0_DQ[54]		DDR1_DQ P[3] /	60] ⁻	DDR1_DQ[31]7 DDR0_DQ[63]		DDR0_DQ[49]/ DDR1_DQ[33]		DDR0 DQS P[6] /	
	BL RS	VD_TP		DDR0_CAS #/ DDR0_CAB	DDR0_BA[1]/ DDR0_CAB	160	[7]/ DDR0_MA[10]		DDR0_MA[4]		DDR1_DQ[17] / DDR0_DQ[49]	DDRO DQS N[6]	DDR1_DQ[19] / DDR0_DQ[51]	54]	DDR1_DQ[24] / DDR0_DQ[56]	P[7]	DDR1_DQ 26] / DDR0_DQ 58]	_			2000 001		
	вк			DDR0_MA[15]	[6]/ DDR0_BA[1]		DDR0_MA[13]/ DDR0_CAB		4]		49]	DDR1_DQS	51]	DDR1_DQ[23] / DDR0_DQ[55]		DDR1_DQ N[3] /	58]	DDR1_DQ 30]/ DDR0_DQ 62]	'9e	DDR0_DQ 51] / DDR1_DQ 35]		DDR0_DQ5	-
		3 800	etin		DDR0_WE #/ DDR0_CAB		13]// DDR0_CAB [0]/ DDR0_MA[13]		DDR0_CS#	eth	DDR1_DQ[DDR0 DQ9 P[6]	DDR1_DQ[DDR0 DQ[55]		DDR0 DQ N[7]	DDR1_DQ			DDR1 DQ[35]		DDR1 DQS N[4]	
112	BJ DH BH	RCO P[1]			[2]/ DDR0_MA[14]				DDR0_CS# [1]	2-	DDR1_DQ[16]/ DDR0_DQ[48]		DDR1_DQ[18]/ DDR0_DQ[50]		DDR1_DQ[25]/ DDR0_DQ[57]		DDR1_DQ 27J7 DDR0_DQ 59]			<u></u>	DDR0_DQ[54]/ DDR1_DQ[38]		5.
JUGEI	BG				14]/ DDR0_CAA [9]/ DDR0_BG[1]		6	stine	DDR0_ALE RT#		DDR0_DQ[21] / DDR0_DQ[37]		DDR0_DQ[18] / DDR0_DQ[34]		DDR0_DQ[28] / DDR0_DQ[44]	0	DDR0_DQ 29] / DDR0_DQ 45]		RSVD_TP		DDR0_DQ[43]/ DDR1_DQ[11]		dunc
	BF DDF M	R_RCO P[0]		6]7 DDR0_CAA [2]7 DDR0_MA[6]		ned						DDR0_DQ9 P[2] / DDR0_DQ9 P[4]		DDR0_DQ[23] / DDR0_DQ[39]		DDR0_DQ N[3] / DDR0_DQ N[5]	5	DDR0_DQ[30] / DDR0_DQ[46]		DDR0_DQ(47] / DDR1_DQ(15]	1 N N T	DDR0_DQS P[5] / DDR1_DQS P[1]	
	BE			20	DDR0_MA[15] /		DDR0_MA[DDR0_CKE [2]		DDR0_DQ[16] / DDR0_DQ[32]	DDR0_DQ5	DDR0_DQ[19] / DDR0_DQ[35]	DDR0_DQ[DDR0_DQ[25] / DDR0_DQ[41]	DDR0_DQ	DDR0_DQ 27] / DDR0_DQ 43]		26		DDR0_DQ[46]/ DDR1_DQ[14]	DDR0_DQ5	
	BD BC DDF	R RCO	6.		DDR0_DA 15] / DDR0_CAA [8]/ DDR0_ACT #	DDR0_CKP	DDR0_CAA [7]/ DDR0_CAA [7]/ DDR0_MA[11]	DDR0 CKE			DDR0_DQ[N[2] / DDR0_DQ9 N[4]	DDR0_DQ[201/	DDR0_DQ[22]/ DDR0_DQ[38]		P[3] / DDR0_DQ P[5]	DDR0_DQ	DDR0_DQ[31]/ DDR0_DQ[47]	nuo.	DDR0_DQI 41]/ DDR1_DQI 9]			
	BB BB	R RCO P[2]	DDR0_MA[3]	DDR0_CKN [0]	DDR0_MA[2]/ DDR0_CAB [5]/ DDR0_MA[2]			DDR0_CKE [1]	DDR0_CKE	9e.	DDR0_DQ[17] / DDR0_DQ[33]		DDR0_DQ[20] / DDR0_DQ[36]		DDR0_DQ[24] / DDR0_DQ[40]		DDR0_DQ 26] / DDR0 DQ 42]				DDR0_DQ[44] / DDR1_DQ[12]		
Indefi	ва		21	DDR0_CKP	DDRO_MA[2]	DDR0_CKN		00		DDR0_MA[12]/ DDR0_CAA					VDDQ	6-	VDDQ		VDDQ		VDDQ		ed un
	AY			[I]			DDR0_MA[DDR0_MA[[6]/ DDR0_MA[12]	DDR0_MA[7e.								
	AW	E	DR0_CS# [0]	DDR0_MA[DDR0_CKE [3]	DDR0_RAS	5]7 DDR0_CAA [0]7 DDR0_MA[5]	DDR0_BA[7]7 DDR0_CAA [4]/ DDR0_MA[7]		DDR0_CAA [1]/ DDR0_MA[9]		DDR1_VRE F_DQ		VCCIO_DD R		VCCIO_DE R		VCCIO_DE R		VCCIO_DD R		
	AV VI	DDQ	ŝ	0]7 DDR0_CAB [9]7 DDR0_MA[0]	5	# 7 DDR0_CAB [3]/ DDR0_MA[16]		2]7 DDR0_CAA [5]7 DDR0_BG[0]		DDR0_MA[DDR0_CAA [3]/ DDR0_MA[8]	60					VCCIO_DI R		VCCIO_DD	und	VCCIO_DD		VCCIO_DD R	
		DDQ	10-	DDR0_DQ[15]		DDR0_DQ[10]		DDR1_DQ[5]7 DDR0_DQ[21]	DDR1_DQ[DDR1_DQ[0]7 DDR0_DQ[16]	DDR1_DQ[VCCGT	VCCGT	VCCGT	lue,	VCCGT	VCCGT		VCCGT	
de	AR AP		DR0_DQ[14]	DDR0_DQS N[1]	DDR0_DQ[11]	DDR0_DQS P[1]		DDR1_DQS P[0] / DDR0_DQS	DDR1_DQ[4]7 DDR0_DQ[20]	DDR1_DQ9 N[0] / DDR0_DQ9	DDR0_DQ[17]		DDR_VREF _CA			~e0					 	_	2 U
3 un	AN	1	DDR0_DQ[13]		DDR0_DQ[12]			P[2]	DDR1_DQ[2]7 DDR0_DQ[18]	N[2]	DDR1_DQ[3]7 DDR0_DQ[19]		DDR0_VRE F_DQ		VCCGT	VCCGT	VCCGT		VCCGT	VCCGT		VCCGT	nec
	AM AL	1	DDR0_DQ[7]	DDR0_DQ[9]	DDR0_DQ[6]	DDR0_DQ[8]		DDR1_DQ[6]7 DDR0_DQ[22]	DDR1_DQ[9]7	DDR1_DQ[7]7 DDR0_DQ[23]	DDR1_DQ[8]7			<u>,</u> d .							ed ut		
		DDQ	7]	DDR0_DQ[2]	6]	DDR0_DQ[3]		DDR1_DQ[12]7 DDR0_DQ[28]	9]7 DDR0_DQ[25]	DDR1_DQ[13]/ DDR0_DQ[29]	8]7 DDR0_DQ[24]				VCCGT	VCCGT	VCCGT		VCCGT	VCCGT		VCCGT	
	AJ		DRO_DQS P[0]		DDR0_DQS N[0]				DDR1_DQS N[1]/ DDR0_DQS N[3]		DDR1_DQS P[1]/ DDR0_DQS P[3]		VCCGT					sine	0				
ed und	stine								ned	01.						6	uno						
d uno							<u>,</u> 5	ugei							def	ine							ined
						<i>defin</i>								ed l							<i>.d</i>	JUUOC	
			Datas	heet, V	olume	1 of 2							9e1.							defi	173		
			nde	stine							Define								ed u				
	efin									unc			vccer					Perr.					ined
1	elli								in								9						

U/U-Quad Core/YProcessor BallInformation Figure 9-7. Y-Processor Ball Map (Upper Left, Columns 64-44)



qe,,			nte			unde	tine					ned	-9e	finer							fined	Un
		íí)	nte		ned						1 of	ned	U/U	J-Quad	l Core/	YProc						
			ire 9-						(110)								ed u	ndef				
BI	43 P	42 VDDQ	41	40 VDDQ	39	38	37	36	35	34 VDDO	33	32 VDDQ	31	30	29	28	27	26 VDDQ	25	24 VDDQ	23	8
ndefille	DDR0_D Q[52] / DDR1_D Q[36]		DDR0_D Q[57] / DDR1_D Q[41]		DDR0_D Q[59] / DDR1_D Q[43]		DDR1_B A[2]7 DDR1_C AA[5]/ DDR1_B G[0]		DDR1_M A[14] / DDR1_C AA[9]/ DDR1_B G[1]		DDR1_C KE[0]	DDR1_M	DDR1_M A[9]7 DDR1_C AA[1]7 DDR1_M A[9]	stine			DDR1_D Q[33] / DDR1_D Q[17]		DDR1_D Q[36] / DDR1_D Q[20]		DDR1_D Q[45] / DDR1_D Q[29]	d une
BN	M DDR0 D	DDR0_D Q[56] / DDR1_D Q[40]		DDR0_D QSN[7]/ DDR1_D QSN[5]	ineo		DDR1_M	DDR1_C KP[0]		DDR1_M A[15] / DDR1_C AA[8]/ DDR1_A CT#		A[6] / DDR1_C AA[2] / DDR1_M A[6]	Ulli	DDR1_C S#[0]		DDR1_D Q[32]/ DDR1_D Q[16]		DDR1_E QSP[4], DDR1_E QSP[2]		DDR1_C Q[40] / DDR1_C Q[24]		
BI		DDR0_D	DDR0_D Q[61] / DDR1_D Q[45]	DDR0 D	DDR0_D Q[62] / DDR1_D Q[46]		A[8]/ DDR1_C AA[3]/ DDR1_M A[8]		113	ned '				DDR1_M		DDR1_D	DDR1_D Q[37]/ DDR1_D Q[21]	nde DDR1	DDR1_[Q[35] / DDR1_[Q[19]	DDR1_D	DDR1_D Q[44] / DDR1_D Q[28]	
Bł		Q[60] / DDR1_D Q[44]	DDR0_D	OSP[7]/ DDR1_D QSP[5]	DDR0_D		DDR1_M A[12]/	DDR1_C KN[0]	DDR1_M A[11]/	DDR1_M A[4]		DDR1_C KE[1]		A[5]7 DDR1_C AA[0] / DDR1_M A[5]		Q[34] / DDR1_D Q[18]	DDR1 D	QSN[4], DDR1_[QSN[2]	DDR1_D	Q[41]/ DDR1_D Q[25]	DDR1_D	50.
unde ^f B: Br	Q[39]		Q[58] / DDR1_D Q[42]		Q[63] / DDR1_D Q[47]		A[12]/ DDR1_C AA[6]/ DDR1_M A[12]		DDR1_M A[11]/ DDR1_C AA[7]/ DDR1_M A[11]		DDR1_C S#[1]		DDR1_M A[3]	DDR1_C KE[3]			Q[39]7 DDR1_D Q[23]		Q[38]/ DDR1_C Q[22]		Q[43] / DDR1_D Q[27]	ed un
во	G DDR0_D Q[42]/ DDR1_D Q[10]		DDR0_D Q[34] / DDR1_D Q[2]	.ndf	DDR0_D Q[38] / DDR1_D Q[6]		DDR1_M A[13]/ DDR1_C AB[0]/ DDR1_M A[13]	DDR1_M	DDR1_M A[10] / DDR1_C AB[7]/ DDR1_M A[10]		DDR1_C KE[2]	stine	DDR1_M A[7]/ DDR1_C AA[4]/ DDR1_M A[7]				DDR1_D Q[52]		DDR1_E Q[50]	a un	DDR1_D Q[61]	
BF		DDR0_D Q[36] / DDR1_D Q[4]	Ined	DDR0_D QSP[4]/ DDR1_D QSP[0]			DDR1 C	DDR1_M A[0] / DDR1_C AB[9]/ DDR1_M A[0]	¢	DDR1_R AS# 7 DDR1_C AB[3]/ DDR1_M A[16]	une	DDR1_C KP[1]		DDR1_M A[2]7 DDR1_C AB[5]/ DDR1_M A[2]		DDR1_D Q[48]	60	DDR1_E QSP[6]		DDR1_C Q[56]		
BE	E DDR0_D Q[45]/ DDR1_D Q[13]		DDR0_D Q[39] / DDR1_D Q[7]	DDR0 D	DDR0_D Q[35] / DDR1_D Q[3]		AS#/ DDR1_C AB[1]/ DDR1_M A[15]								0	nde	DDR1_D Q[53]		DDR1_C Q[54]		DDR1_D Q[60]	711
UNOBE		DDR0_D Q[37] / DDR1_D Q[5]	DDR0_D	QSN[4]/ DDR1_D QSN[0]	DDR0_D	,O	DDR1_W E#/	A[1]7 DDR1_C AB[6]/ DDR1_B A[1]		DDR1_A LERT#	DDR1_B A[0]7 DDR1_C	DDR1_C KN[1]	DDR1_M A[1]/ DDR1_C	DDR1_P AR	NG -	DDR1_D Q[49]		DDR1_C QSN[6]		DDR1_C Q[57]	0°	led un
BC BE BA	C Q[40] / DDR1_D Q[8] 3		Q[32] / DDR1_D Q[0] VDD0	d	Q[33] / DDR1_D Q[1]		DDR1_C AB[2]/ DDR1_M A[14]		DDR1_0 DT[0]		DDR1_C AB[4]/ DDR1_B A[0]	stin	DDR1_C AB[8]/ DDR1_M A[1]		VDDQ		DDR1_D Q[51]		DDR1_E Q[55]	ed u	DDR1_D Q[59] TP5	
AN AV AN	VCCIO_D DR	VCCIO_D DR	VCCIO_D DR	VCCIO_D DR	VCCIO_D DR	VCCIO_D DR	VCCIO_D DR	VCCIO_D DR	VCCIO_D DR	VCCIO_D DR	VCCIO_D DR	VCCIO_D DR	VCCIO_D DR	VCCIO_D DR	VCCIO_E DR	VCCIO_E DR	VCCIO_L DR	VCCIO_I DR	D			
AL AT AF	r vccgt		VCC VCC	VCC		VCC VCCG1	ci N C	VCC	VCC VCCG1		VCC	VCC VCC		VCCSA_ DDR	VCCSA_ DDR VCCSA	undi		VCCIO VCCIO		VCCIO_S ENSE VSSIO_S ENSE	VCCHDA	ned u
	м		VCC VCC			VCCG1 VCCG1	00-		VCCG1 VCCG1			VCC VCC	-0 ¹	VCCSA	VCCSA VCCSA			VCCIO VCCIO			VCCSRA M_1P0 VCCSRA M_1P0 VCCSRA	nee
	VCCGT		VCC	d vi ^r	967.	VCCG1			VCCG1		Jur	VCC		VCCSA	VCCSA			VCCIO	defi		M_1P0]
	2	und	efili						, nd									ad u				
und	etinec						-9e	tined							tine	Jun						red
20					1 cfl	ned	UI.						ned	unde						6-	unde	
	efined	174		ed u	nor						du	ndefi				D	atashee	et, Volu	me 1 o	f 2		stined "
		d un	9em						un un	defin								led .				
2	etine							ane	0							dun	•					



				d un								und ^e								enn				
		.06	Fig	ure 9	-9.	Y-Pr	oces	sor B	all M	ap (L	, co Ipper	Riał	nt <i>.</i> Co	lumr	ıs 42	-1)			9 UI.					
-	0	22	21	20	19	18	17	16	15		13	12	11	10	9	8	7 GPP_A5/ LFRAME#	6	5 GPP_A4 /	4	3	2	1	
Yelli.	BP		DDR1_DQ[42]/	DRAM_RE SET#	RTCX1	RTCX2	PROC_POF	PCH_OPIR COMP	DSW_PWR	Ōĸ		RTCRST#	SLP_LAN#	SLP SUS#	WAKE#	GPP_A6 / SERIRQ	ESPI_CS#		GPP_A4 / LAD3 / ESPI_IO3	GPP_A16/ SD_1P8_S EL	RSVD RSVD		TP4	UNO
	BM DI	DR1_DQ SN[5]/	DDR1_DQ[26]				IRCOMP	0.	ОК						<u>defi</u>	SERIRQ				EL -	1010			
	BL	SN[3]	DDR1_DQ[47] / DDR1_DQ[HDA_RST # / I2S1_SCL	no	HDA_SDI1		HDA_SDI0			I2S1_SFR		GPP_A0 / RCIN#	•			GPP_A13/ SUSWARN #/		GPP_A17/ SD_PWR_ EN_#/ ISH_GP7	GPP_A21/ ISH_GP3	100		
	вк об	DR1_DQ SP[5] /	31]		K	HDA_BLK	I2S1_RXD	HDA ₇ SDO	1250 <u>_</u> RXD	I2S1_TXD			GPP_A1 / LAD0 / ESPI_IO0					# / SUSPWRD NACK		ISH_GP7			-	
		SP[3]	DDR1_DQ[0	HDA_SYN	К		12S0_TXD			, ed	RSMRST#	ESPI_IO0			GPP_A2/		GPP_A14 / SUS_STAT	10	Sx_EX- IT_HOLDC FF#/ GPP_A12/ BM_BUSY) GPP 422/		GPP A20/	
	BJ	n,	46] / DDR1_DQ[30]		HDA_SYN C / I2S0_SFR M		TP2	GPD9 /	TP1	Je	11.	KSMIKST#	CDD 40 (GPP_A9 / CLKOUT_L PC0 / ESPI_CLK		GPP_A2/ LAD1/ ESPI_IO1		GPP_A14/ SUS_STAT #/ ESPI_RES ET#		BM_BUSY #/ ISH_GP6	GPP_A22/ ISH_GP4		GPP_A20/ ISH_GP2	
1ip	BG		DDR1_DQ[58]		INTRUDER #	SRTCRST#	¥	SLP_WLAN #	10	SLP_S5#			GPP_A8 / CLKRUN#	GPP_A3 / LAD2 / ESPI_IO2			JAC							Śn.
unde.	BF D	DR1_DQ SN[7]				RSVD		GPD5 / SLP_S4#	GPD2 /	GPD3 / PWRBTN#			GPP_A18/ ISH_GP0	25/1_102	GPP_A15/ SUSACK#	ne	GPP_A11 / PME#	r	GPP_A10 / CLKOUT_LP C1	•	GPP_A7 / PIRQA#		SD_RCOM	20.
	BE BD	DR1_DQ	DDR1_DQ[63]		RSVD	RSVD	GPD6 / SLP_A#	GPD0 / BATLOW#	LAN_WAK E#	GPD1 / ACPRESEN				GPP_B7 / SRCCLKRE Q2#	,000	GPP_B3 / CPU_GP2		GPP_B2 / VRALERT#		GPP_A23/ ISH_GP5	1	GPP_A19/ ISH_GP1	1	
	вс		DDR1_DQ[62]		RSVD	C. L. L			GPD11/ LANPHYPC				GPP_B4 / CPU_GP3	Q2#	GPP_B12/ SLP_S0#	2.0_0/2	GPP_B11/ EXT_P- WR_GATE #		GPP_B10 / SRCCLKREQ 5#		GPP_B15/ GSPI0_CS #	A A M	EMMC_RC OMP	
	вв				<u> </u>	RSVD		GPD7 / RSVD		RSVD		GPP_B1 / CORE_VID 1	<u>,</u>	GPP_B5 / SRCCLKRE Q0#		GPP_B13/ PLTRST#		GPP_B23/ SML1ALER T# / PCHHOT#		GPP_B18/ GSPI0_MC SI		GPP_B19/ GSPI1_CS #	5	
	BA AY	TP6	RSVD	RSVD	RSVD	RSVD TP	RSVD_TP		GPD8 / SUSCLK	GPD4 /	GPP_B0 / CORE_VID 0										_			
	AW									100.		GPP_B20/ GSPI1_CL K		GPP_B16/ GSPI0_CL K	GPP B6 /	GPP_B22/ GSPI1_MO SI	GPP B9 /	GPP_B17/ GSPI0_MI SO	GPP B8 /	GPP_B21/ GSPI1_MI SO		VCCPGPPE		
defi	AV V AU	CCHDA				DCPRTC		10	VCCSPI		SPI0_IO3	SPI0_MIS	SPI0_IO2	SPI0_CLK	GPP_B6 / SRCCLKRE Q1#	SPI0_CS2	GPP_B9 / SRCCLKRE Q4#	SPI0_CS1	GPP_B8 / SRCCLKREC 3#	SPI0_CS0	GPP_B14/ SPKR	VCCPGPPA	VCCPGPPB	d un
U	AT		VCCPRIM_ 1P0		VCCRTC	DCPRTC	, ur	VCCPRIM_ CORE	VCCSPI		GPP_F1 / I2S2_SFR M		GPP_F0 / I2S2_SCL K		GPP_F11/ I2C5_SCL / ISH_I2C2_ SCL		GPP_F7 / I2C3_SCL		GPP_F3 / I2S2_RXD		SPI0_MOS		VCCPGPPA	5
	AR AP		VCCPRIM_ 1P0		VCCRTC	2		VCCPRIM_ CORE			VCCPGPPG		GPP_F2 / I2S2_TXD		GPP_F14/ EMMC_DA TA1		GPP_F5 / 12C2_SCL		GPP_F6 / I2C3_SDA		GPP_F4 / 12C2 SDA		VCCPGPPF	
	AN			2					VCCPGPPG			GPP_F13/ EMMC_DA TAO	1232_170	GPP_F15/ EMMC_DA TA2	TA1	GPP_F20 / EMMC_DA TA7	1202_300	GPP_F9 / I2C4_SCL	1203_30A	GPP_F8 / I2C4_SDA		VCCPGPPF		
	АМ			IU60							VCCDSW_ 3P3	<i>d v</i>	GPP_F12/ EMMC_CM D		GPP_F17/ EMMC_DA TA4		GPP_F10 / I2C5_SDA J ISH_I2C2_ SDA	-	USB2P_2	SUC.	USB2N_2		DCPDSW_ 1P0	
	AL	2	VCCPRIM		VCCRT- CPRIM_3P 3 VCCRT-	VCCPRIM_ 1P0			VCCDSW_ 3P3	, nd	61.	GPP_F18 / EMMC_DA TA5		GPP_F21/ EMMC_RC LK		GPP_F22 / EMMC_CL K		USB2N_3	<i>U</i> o	USB2P_3		DCPDSW_ 1P0		
a undef	AK AJ		VCCPRIM_ 3P3		3 3	1P0		6	ner	Q.		GPP_F19/ EMMC_DA TA6		GPP_F16/ EMMC_DA TA3		GPP_F23	.6 0	USB2N_1		USB2P_1		VCCPGPP(
JUNOS	L							nde					•		2	etin							12	led .
							red								Unc							76.	'961.	
					n.	9ein							26	ine										
												, d V								und	<u>S</u> ,			
										d un														
Inde	311.							20	stine															. 60
d V							6	une							n,	961.							defi	IUC
						Jeti																du	,n-	
			Data	sheet	Volum	e 1 of 3	7						Inde	31.							lefin	75		
			2010	e	onann	01 4	_													y nu	1/	-		
			unu	sheet,				unde			uger,								stine					ined "
	ell	765							a n	29 v							6	uns						

U/U-Quad Core/YProcessor BallInformation Figure 9-9. Y-Processor Ball Map (Upper Right, Columns 42-1) 21 20 19 18 17 16 15 14 13 12 11 10 0 0



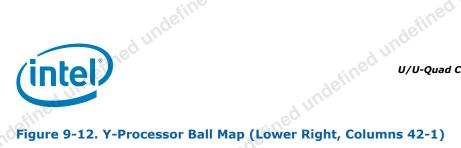
den					und	etine	,						efin	ed						j.	ned u	
	Ú	nte		ned							fine	d un	1/U-Qı	iad Co	re/YPı	rocess	or Ball	Inforn				
									red	undi							und	lefil,				
64	63	re 9-: 62	10. Y	'-Pro 60	59	58 DDR1	II Ma 57	56 DDR1	55	Left, 54	53	mns 6 52	51 51	50	49	48	47	46	45	44	1	
NDOC AH VDDC	2	DDR0_ DQ[4]		DDR0_ DQ[1]	į	DQ[10] / DDR0_ DQ[26]		DQ[11] / DDR0_ DQ[27]						1	1						ined	JUUO
AG	DDR0 DQ[5]	C	DDR0_ DQ[0]	ined			DDR1_ DQ[15] / DDR0_ DQ[31]		DQ[14] / DDR0_ DQ[30]]	VCCGT	d un	loc .	Vecet	Vecet		NCCCT	VCCGT		VCCGT		
AE AD <mark>VCCG</mark> AC	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT		VCCGT	VCCGT VCCGT	VCCGT		VCCGT	VCCGT	0	VCCGT		
AB VCCG AA Y VCCG W		VCCGT VCCGT		VCCGT VCCGT	VCCGT	VCCGT VCCGT	VCCGT	VCCGT VCCGT	VCCGT	VCCGT VCCGT	VCCGT		VCCGT	VCCGT	VCCGT	sine	VCCGT	VCCGT		VCCGT		
V VCCG U T R	T VCCGT VCC	VCCGT \	VCCGT VCC	VCCGT	VCCGT	VCCGT	VCCGT VCC	VCCGT	VCCGT	VCCGT VCCGT	VCCGT		VCCGT VCCGT	VCCGT	VCCGT		VCCGT	VCCGT		VCCGT	6-	und
P VCC		VCC		VCC	d un	VCC		VCC				VSSGT _SENS E VCCGT	ndei	VICCOT		NCCCT		NCCCT		VCCGT	tinec	
N M VCC L	VCC VCC	vcc	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	-SENS E VCC	VCC	VCCGT VCC	VCC	VCCGT	VCC	VCCGT	VCC	VCC		
к ј <mark>VCC</mark> н	VCC	C		CFG[12]	CFG[15	CFG[13		CFG[19]	CFG[4]	CFG[16	CFG[3]	CFG[2]	BPM#[0]	BPM#[1]	CATER R#	PROCH OT#	THERM TRIP#	EDP_T XN[2]	EDP_T XN[0]	EDP_T XN[1]		
G F VCC		C	CFG[11			CFG[9]	neò	CFG[18]	CFG[7]	CFG[17	CFG[1]	CFG[0]	BPM#[2]	BPM#[3]	PECI	PROC_ TDO	PROC_ TRST#	EDP_T XP[2]	EDP_T XP[0]	EDP_T XP[1]		
D VCC		C	CFG[8]		PROC	ndei	CFG[10		CFG[5]	PROC	PROC_ TCK	РСН Т	PROC_ PRDY#	PCH_JT AG_TD	RSVD	DDI1	DDI1 TXP[3]	DDI1	DDI1_ TXP[2]	DDI2	etined	
C B VCC		SKTOC C#	VCCST _PWRG D	etin	STMS	VIDALE RT#		CFG[6]	PROC_	TDI	PCH_JT AG_TC K	RST#	PCH_JT AG_TD O		JTAGX	TXN[1]	DDI1_	TXP[0]	DDI1_ TXN[2]	TXP[1]		
A VCC		PROCP WRGD). O.	ITP_PM ODE		VIDSO UT		VIDSC K		CFG_R COMP	0	PCH_JT AG_TM S		eDP_R COMP		DDI1_ TXP[1]		DDI1_ TXN[0]		DDI2_ TXN[1]		
A Vcc	unoe							und														
undefin.						nde	fine						2	efine	,d 0.							ed u
				16 ^{fi}	ned							ined	unu							d un	9em	
			d un							-01	Inde							ind	Stine			
	d und	S _I II.						27.								76						
indefine						2	etine								ed u							.01
ed U.					ned	unu							d un	9er.							defin	
	176		d U	ndei							. ndf	stine				Data	-boot \	(olumo				
A Vcc	110	Jefin								ined						Datas	sincel, V	volutite	J UI Z			
efin	ed v.						200	ed u	IUN-						6	unde					define	

led underine U/U-Quad Core/YProcessor BallInformation

(intel) defined un

							cesso																
	AH	43	42	41 VCC	40	39	38 VCCG1	37	36	35 VCCG1	34	33	32 VCC	31	30	29 VCCSA	28	27	26 VCCIO	25	24	23	
detin	AG AF	VCCGT		VCC			VCCG1	11.60		VCCG1			VCC		VCCSA	VCCSA		VCCPLL _OC	VCCIO	1	VCCIO		JUNC
	AE			VCC	VCC		VCC		VCC	VCC		VCC	VCC			VCCSA		VCCPLL _OC	VCCIO	1	VCCIO	VCCIO	
	AD AC	VCCGT		VCC		160	VCCG0			VCCG0			VCC	γ_{I} ,	VCCSA	VCCSA			VCCST		VCCIO	VCCIO	
	AB			70	90.							3							VCCST	0		VCCSR AM_1P	
	AA Y	VCCGT		VCC VCC			VCCG0 VCCG0			VCCG0 VCCG0	ن .		VCC VCC		VCCSA	VCCSA VCCSA		-	G VCCST			VCCCL K3	
	w	VCCGI	e, i, i,							nite.	6				VCCJA			6					
	V U	,		VCC		ļ	VCCG0		V V.	VCCG0			VCC		-	VCCSA	9er		VCCST		_	VCCCL K3	
defil	Т	VCCGT		VCC			VCCG0	sine		VCCG0			VCC		VCCSA	, O		VCCPLL	VCCST G VCCST				d unc
JUL	R P			VCC			VCCG0	5		VCCG0			VCC	Ó	0	VCCSA			G			VCCCL K5	30
	N		VCC		VCC	neo	VCC		VCC		VCC		VCC	Un	VCCSA		VSSSA _SENS E						
	м	VCC		VCC	uge.	VCC		VCC		VCC		VCC	1n-	VCCSA		VCCSA _SENS E		RSVD		RSVD	0	RSVD	
	L		VCC	ed	VCC		RSVD		RSVD		VCC_S ENSE		VSS_S ENSE		VCCSA		RSVD		RSVD		RSVD		
	к J		EDP_A UXN		DDI2_ AUXN		CLKOU T_PCIE _N3		CLKOU T_PCIE _N2	Yeti	CLKOU T_ITPX DP_N		CSI2_D N3		CSI2_D N2	•	PCIE9_ TXP	10 ⁰	PCIE7 TXP / SATA0		PCIE5_ TXP		
		d UN	UXN		AUXN	CLKOU		CLYOU		CLKOU	DP_N		N3				96.		TXP		ТХР		
defi	н	EDP_T XN[3]		DDI1_ AUXN		T_PCIE _N5		CLKOU T_PCIE _N4	20	T_PCIE _N1		CSI2_D P1		CSI2_C LKN0		CSI2_D N0		PCIE10 _TXP		PCIE8 TXP / SATA1 A_TXP		PCIE6_ TXP	JUN
Une	G		EDP_A UXP		DDI2_ AUXP	<	CLKOU T_PCIE _P3	0	CLKOU T_PCIE _P2		CLKOU T_ITPX DP_P		CSI2_D P3		CSI2_D P2		PCIE9_ TXN		PCIE7 TXN / SATA0_ TXN		PCIE5_ TXN	10fil	ler.
		FDP T		וזסס		CLKOU	1	CLKOU		CLKOU	DP_P	CSI2_D		11				PCIE10		PCIE8 TXN /		00	
	F	EDP_T XP[3]		DDI1_ AUXP	nde	CLKOU T_PCIE _P5		CLKOU T_PCIE _P4		CLKOU T_PCIE _P1		N1	stine	CSI2_C LKP0		CSI2_D P0		PCIE10 _TXN		SATA1		PCIE6_ TXN	
	E D	DDI2_T XP[3]		DDI2_T XP[2]		CSI2_C LKN3		CSI2_D N10		CSI2_D N8	6	CSI2_D N7		CSI2_C LKN1		CSI2_D N4		PCIE10 _RXP	Unc	PCIE8 RXP / SATA1 A_RXP	-	PCIE6_ RXP	
		XP[3]	96.			LKN3					neu							_RXP		A_RXP		RXP	
	С	ed n	DDI2_T XP[0]				CSI2_D N11		CSI2_D N9	U0-	CSI2_C LKN2		CSI2_D N5		CSI2_D N6		PCIE9_ RXN	() ·	PCIE7 RXN / SATA0_ RXN	-	PCIE5_ RXN		
. de	в	DDI2_T XN[3]		DDI2_T XN[2]		CSI2_C LKP3		CSI2_D P10	le.	CSI2_D P8		CSI2_D P7		CSI2_C LKP1		CSI2_D P4	<i></i>	PCIE10 _RXN		PCIE8 RXN / SATA1		PCIE6_ RXN	201
3 Ullis					EDP_DI			80							CSI2 D		PCIE9		DOLEZ	A_RXN	PCIES		nec.
	A		DDI2_T XN[0]		EDP_DI SP_UTI L	1 ne	CSI2_D P11		CSI2_D P9		CSI2_C LKP2		CSI2_D P5	, d U	CSI2_D P6		PCIE9_ RXP		PCIE7_ RXP / SATA0_ RXP	-	PCIE5_ RXP	ndef	
					, nd	e,							efin								leo .		
ed unde												Un							27	9e,			
				<i>(i</i> ,																			
		ed /							2								60.						
.6	SUI															ed	U						2
d une								Uge							. de								finec
														.01								unde	
					n.	ger.							Jefin	10							neo		
			Datas	heet, V	olume	1 of 2	csi2 D Pil			unde		d ur								Uge,	177		tined
			Datas	S1,,							etine												
										uno								Perr,					
3	é	11-							inec	P							d UN						

Jed undefined undefined Figure 9-11. Y-Processor Ball Map (Lower Middle, Columns 43-23)



			nt	el	2							AINE		U/U-Q	uad Co	ore/YP	rocess	or Bal	lInforr	nation			
			ed '							-9	und							d uni	Jefin				
	n,		ure 9		Y-Pr			all Ma		ower	Righ												
AH	22	21 /CCPRIM_ 3P3	20	19 VCCPRIM_ 1P0	18 VCCPRIM_ 1P0	17	16	15 VCCPRIM_ 1P0	14	13 VCCPRIM_ 1P0	12	11 GPP_G1/ SD_DATAC	10 GPP_G6 /	9 GPP_G0 / SD_CMD	8 GPP_G5/	7 RSVD	6 USB2N 9	5 USB2N_5	4 USB2P 9	3 USB2P_5	2 VCCPGPPD		
AF AE				VCCPRIM_ CORE VCCPRIM_ CORE	VCCPRIM_ CORE VCCPRIM_ CORE		VCCATS	VCCATS			GPP_G7 / SD_WP	GPP_G4 / SD_DATA3	SD_CER	GPP_G3 / SD_DATA2	SD_CD#	USB2_ID	USB2_VBL SSENSE	USB2N_7		USB2P_7		VCCPGPPD	<i>U</i> 1.
AD						9.01						GPP_C16/ I2C0_SDA	1	GPP_C23/ UART2_CT S#	GPP C8 /	GPP_C21 / UART2_TX D		GPP_C20/ UART2_RX D	GPP_C13,	GPP_C22, UART2_R S#	-9e	VCCPRIM_ 3P3	
AC							_				GPP_C0 / SMBCLK	117	GPP_C4 / SML0DATA		GPP_C8 / UARTO_RX D	GPP_C14/ UART1_RT	GPP_C12/ UART1_RX D/ ISH_UART 1_RXD	GPP_C15/	GPP_C13, UART1_T2 D/ ISH_UART 1_TXD	ed	VCCPRIM_ 3P3		
AB	v	CCSRAM_ 1P0	ned	VCCAPLL_ 1P0	VCCAPLL_ 1P0		VCCPRIM_ 1P0	VCCPRIM_		0	GPP_C11/ UART0 CT	GPP_C19/ I2C1_SCL	GPP_C10/ UARTO RT	GPP_C18/ I2CI_SDA	GPP_C9 / UART0_TX D	S# / ISH_UART 1_RTS#	GPP_C5 / SMLOALER T#	S# / ISH_UART 1 CTS#	GPP_C6 / SML1CLK	GPP_C17, I2C0_SCL	VCCPGPPE	VCCPGPPE	
Y W	1	VCCCLK4		VCCCLK2	VCCCLK1		IPU	1P0	200		UARTO_CT S# GPP_D21		GPP_C7 / SMLIDATA		GPP_C2 / SMBALERT #		T# GPP_C1/ SMBDATA	0	GPP_C3 / SMLOCLK		VCCMPHYA ON_1P0	_	
N N N	,0	VCCCLK4		VCCCLK2	VCCCLK1		VCCAM- PHYPLL_1F 0	VCCAM- PHYPLL_1P 0	3.			GPP_D20 / DMIC_DAT A0	-	GPP_D16 / ISH_UART 0_CTS# / SML0BALE RT#	#	GPP_D22		GPP_D23/ I2S_MCLK		GPP_D19, DMIC_CLF 0	(((((((((((((((((((VCCMPHYA ON_1P0	
U							<i>'ge,</i>				GPP_D17/ DMIC_CLK 1		GPP_D13/ ISH_UART 0_RXD / SML0BDAT A	20	GPP_D18 / DMIC_DAT AI		GPP_D15/ ISH_UART 0_RTS#	<u></u>	GPP_D14 ISH_UAR1 0_TXD / SML0BCLH	(VCCMPHYO T_1P0	sine	9.0.
T		VCCCLK5		VCCCLK6		30,0	VCCMPHYC T_1P0 VCCAPLLE BB_1P0	VCCMPHYG T_1P0 VCCAPLLE BB_1P0			RSVD	GPP_D12		GPP_D7 / ISH_I2C1_ SDA		GPP_D10		GPP_D11		GPP_D8 / ISH_I2C1_ SCL	nd'	VCCMPHYG T_1P0	
Р				nı,			DD_1PU	DD_1PU		RSVD	CDD EQ./	GPP_D9	GPP_E2/	GPP_D1		GPP_D5 / ISH_I2C0_ SDA		GPP_D6 / ISH_I2C0_ SCL	- CDD D4/	GPP_D3		XCLK_BIA SREF	
N	٦	RSVD		RSVD		RSVD		RSVD		00		GPP_E10/ USB2_OC:	SATAXPCIE 2/ SATAGP2	GPP_E7 / CPU_GP1	GPP_D2	GPP_E15 / DDPD_HPD	GPP_D0	GPP_E22	GPP_D4 / FLASHTRI G		USB2_COM P	1 XTAL24_IN	
L I	RSVD	<u>Ino.</u>	RSVD		RSVD		RSVD			8	RSVD	Ŧ	GPP_E14/ DDPC_HPD 1		GPP_E6 / DEVSLP2	2	GPP_E18 / DDPB_C- TRLCLK		GPP_E23		XTAL24_C		-
J PCI	TIE3_TXP		PCIE1_TXP USB3_5_T XP	PCIE2_TXP	USB3_3_T XP		USB3_1_T XP					GPP_E1 / SATAXPCII 1/ SATAGP1										SYS_PWRO K	ں د
н		CIE4_TXP	PCIE1_TXN	USB3_6_T	USB3 3 T	USB3_4_T	<u> </u>	USB3_2_T XP/ SSIC_TXP			RSVD	GPP_E0 /	GPP_E5/ DEVSLP1		GPP_E8 / SATALED#		GPP_E19 / DDPB_C- TRLDATA		GPP_E20, DDPC_C- TRLCLK		SYS_RESE T#	aine	0
G PCI	IE3_TXN	CIE4_TXN	USB3_5_T XN	PCIE2_TXN USB3_6_T XN	USB3_3_T XN	USB3_4_T	USB3_1_T XN	USB3_2_T XN/ SSIC_TXN			CL_CLK	SATAGPO	GPP_E4 / DEVSLP0	01.	GPP_E11/ USB2_OC2 #		GPP_E16 / DDPE_HPE 3	, ,	GPP_E21 / DDPC_C- TRLDATA	RSVD	Unc	RSVD	
E					0							GPP_E3 / CPU_GP0			#		3						
D C PC	CIE3_RX	CIE4_RXP	PCIE1_RX N/	USB3_6_R XP	USB3_3_R	USB3_4_R XP	USB3_1_F	USB3_2_R XP / SSIC_RXP		eit.	CL_DATA	GPP_E13/ DDPB_HPD							N N	eDP_VDDI N			
в	N F	PCIE4_RX	USB3_5_R XN	PCIE2_RX N/ USB3_6_R XN		USB3_4_R XN		USB3_2_R XN / SSIC_RXN	nu l	Je.	CL_RST#	0	PCIE_RCO		GPP_E12/ USB2_OC3		eDP_BKLC		RSVD	RSVD			-
	IE3_RXP		PCIE1_RXP / USB3_5_R XP		USB3_3_R XP		USB3_1_R XP	sine				CSI2_COM	1	PCIE_RCO MPN		GPP_E17/ EDP_HPD							
						6	uno							nr.	Jein							defin	
						INEC								3. 0.							d un		
				edv	ILC.						2	unde	5						6	efin			
undef			Jefil							2011								ined	U				
									d ut								nde						
undei								Jefin								led)							, ed
						e	Jun							JUN								ndefi	
					nde	SUL.						2	etine								ed v		
		178		ned'	0.							unc					Data	sheet,	Volume	e 1 of 2			
											ine							sine					
undef	sine								ed	Ju-							unde					Idefin	



und^{efined un}

	undefine		def	ined			defined
	U/U-Quad Core/YProcessor BallInfor	mation	Idefined undef		(ir	itel	
2					d und	31 31	
Ball #	Table 9-2. Y-Processor Ball Ball Name	LIST (Sneet 1	Interleaved (IL)	Non-Interleaved	X [um]	Y [um]	
	CC12 COMP			(NIL)			
A11	CSI2_COMP			kine.	6763.51	-7541.01	ed
A14	VSS		nde		6119.37	-7541.01	YetIII.
A16	USB3_1_RXP		ed v		5475.22	-7541.01	
A18	USB3_3_RXP PCIE1_RXP / USB3_5_RXP		ACTIN		4831.08	-7541.01	
A20			nor		4186.94	-7541.01 -7541.01	
A22	PCIE3_RXP	ed			3542.79		
A24	PCIE5_RXP	efili			2898.65	-7541.01	
A26	PCIE7_RXP / SATA0_RXP	JULY		der	2254.5	-7541.01	
A28	PCIE9_RXP			dui	1610.36	-7541.01	
A30	CSI2_DP6			sino	966.22	-7541.01	. ner
A32	CSI2_DP5		0,,,0		322.07	-7541.01	defin.
A34	CSI2_CLKP2		edv		-322.07	-7541.01	
A36	CSI2_DP9		- activity		-966.22	-7541.01	
A38	CSI2_DP11		una		-1610.36	10.	
A40	EDP_DISP_UTIL	ed.			-2254.5	-7541.01	
A42	DDI2_TXN[0]	efill			-2898.65		
A44	DDI2_TXN[1]	unc		uqe,	-3542.79	-7541.01	
A46	DDI1_TXN[0]	0		d Un	-4186.94		
A48	DDI1_TXP[1]			sine	-4831.08		
A5	VSS				8401.05	-7541.01	YetII.
A50	eDP_RCOMP		ed v		-5475.22		un
	PCH_JTAG_TMS		10 fille			-7541.01	
A54	CFG_RCOMP		inos		-6763.51	20.	
A56	VIDSCK	ed			-7407.66	×	
A58	VIDSOUT	Jefin.			-7953.09		
A60	ITP_PMODE	uno		de	-8401.05		
A62	PROCPWRGD	eo		d UI	-8855.71		
A64	vcc			fine -	-9310.37		
A7	GPP_E17 / EDP_HPD			ge.	7946.39	-7541.01	76till
A9	PCIE_RCOMPN		du		7407.66	-7541.01	undefin
AA10	GPP_C10 / UARTO_RTS#		Jefin'		7067.55	-1932.43	
	GPP_C11 / UARTO_CTS#		unos		6574.79	-1932.43	
	VCCPRIM_1P0		0		5846.1	-1869.71	
AA16	VCCPRIM_1P0	Aefill			5350.8	-1869.71	
0		- un		6	4855.5	-1869.71	
AA19	VCCAPLL_1P0	20 C		du.	4360.2	-1869.71	
AA2	VCCPGPPE			<i>since</i>	9038.59	-1932.43	
AA21	VCCSRAM_1P0			nde.	3864.9	-1869.71	reti
AA23	VCCSRAM_1P0		-0 V	· *	3369.6	-1869.71	, uno-
	Datasheet, Volume 1 of 2	etin	ed undefined t		ined	-1869.71 -1932.43 -1869.71 -1869.71 179	
fined	undefine	red unor		4 und	em		



Table 9-2.

	(intel) red undefine		24	stineu			ned
	thed un		ad uno	-		unden	*
	(Intel)		u/	U-Quad Core/YProc	cessor Ball	Information	
	1 000		nde			efili	
	Aine				JUN		
	Table 9-2. Y-Processor Ball	List (Sheet 2	of 40)				
Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved	X [um]	Y [um]	
	. net			(NIL)			
	VSS			sine	2874.3	-1869.71	
	VCCSTG		born and a second se	6	2379	-1869.71	11
	VSS		du.		1883.7	-1869.71	
	VCCSA		fine		1388.4	-1869.71	
	VSS		nac		893.1	-1869.71	
	vcc	ed	0		397.8	-1869.71	
	VSS	1efille		6	-97.5	-1869.71	
20	VCCG0	una		dei	-592.8	-1869.71	
	VSS	0		d un	-1088.1	-1869.71	
	VCCG0			sinet	-1583.4	-1869.71	
	GPP_C6 / SML1CLK			9e,	8545.83	-1932.43	sinc
-	VSS		du'		-2078.7	-1869.71	
	vcc		sine		-2574	-1869.71	
	vss		nde		-3069.3	-1869.71	
AA44	vss	e e			-3564.6	-1869.71	
AA46	VSS	efine			-4059.9	-1869.71	
AA47	VSS	Inos		-96	-4555.2	-1869.71	
AA49	VSS	e o		4 Une	-5050.5	-1869.71	
AA50	VSS			sinec	-5545.8	-1869.71	
AA51	VSS			ye.	-6041.1	-1869.71	Sin
AA53	VCCGT		-0 ⁰		-6574.79	-1932.43	
AA55	VSS		sine		-7067.55	-1932.43	
AA57	VSS		nde.		-7560.31	-1932.43	
AA59	VSS	0	6		-8053.07	-1932.43	
AA6	GPP_C5 / SML0ALERT#	stine			8053.07	-1932.43	
AA61	VSS	mole		à	-8545.83	-1932.43	
AA63	VSS	ed			-9038.59	-1932.43	
AA8	GPP_C9 / UART0_TXD			cin ^{co}	7560.31	-1932.43	
AB1	VCCPGPPE			den	9310.37	-1610.36	
AB11	GPP_C19 / I2C1_SCL		٨'	<i>N</i> /	6821.17	-1610.36	defin
AB13	VSS		sinec		6328.41	-1605.28	
AB3	GPP_C17 / I2C0_SCL		der		8792.21	-1610.36	
AB5	GPP_C15 / UART1_CTS# /		000		8299.45	-1610.36	
	ISH_UART1_CTS# VCCGT	nip.			-6821.17	-1610.36	
	VCCGT	nder.			-7313.93	-1610.36	
	VCCGT	ed V.		nu i	-7806.69		
	VCCGT	N. C.		ine ⁰	-7806.69	-1610.36	
				ndefill	-8299.45	-1610.36	
	180	1	ned undefined		1	-1610.36 -1610.36 -1610.36	
	d under	indefil			define		
eine				١٢ .	<i>7</i> ~		



Table 9-2.

<page-header><page-header></page-header></page-header>		d under.		indef			105	Ineo
		U/U-Quad Core/YProcessor BallInforma	ation	lefined U.		íí)	ntel)	
Ball # Ball Name LPDDR3 Taterlaved (11) Non-Interliaved (NL) X [um] Y [um] A864 VCCGT		d ^{ur}	nu ,					
Ball # Ball Name LPDDR3 Taterlaved (11) Non-Interliaved (NL) X [um] Y [um] A864 VCCGT	20	Stine .	cined -			dulli		
Lan Relie Lan Series Lansatze Lansatze Kluis Human Kluis Human Human </th <th>uno.</th> <th>Table 9-2. Y-Processor Ball L</th> <th>ist (Sheet 3 o</th> <th>of 40)</th> <th>nig.</th> <th>6°</th> <th></th> <th></th>	uno.	Table 9-2. Y-Processor Ball L	ist (Sheet 3 o	of 40)	nig.	6°		
AP GPP_C14/JUNT1_ETS#/ ISH_UART1_ETS# 7806.69 -1610.36 AP GPP_C4/SML0DTA 7767.55 3288.29 AC10 GPP_C4/SML0DTA 7867.55 3288.29 AC12 GPP_C0/SMBCLK 6574.73 4288.29 AC15 VSS 5846.1 -1310.91 AC16 VSS 350.8 -3310.91 AC18 VSS 4455.5 -3130.91 AC19 VSS 4455.5 -3130.91 AC19 VSS 9038.59 -1288.29 AC2 VCCRIM_SP3 9038.59 -1288.29 AC2 VCCI0 2874.3 -1310.91 AC2 VCCI0 2874.3 -1310.91 AC2 VCCI0 2874.3 -1310.91 AC2 VCCGG 2874.3 -1310.91 AC2 VCCGG 97.8 -1310.91 AC2 VCCG 97.8 -1310.91 AC2 VCC 97.8 -1310.91 AC29 VCCSA -97.5 <th>Ball #</th> <th>Ball Name</th> <th>LPDDR3</th> <th>Interleaved (IL)</th> <th>Non-Interleaved (NIL)</th> <th>X [um]</th> <th>Y [um]</th> <th></th>	Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]	
AB9 GPP_C18 / 12C1_SDA 7313.93 1610.36 AC10 GPP_C4 / SNLDDATA 7667.55 1288.29 AC12 GP_C0 / SMBCLK 6574.79 1288.29 AC15 VSS 550.8 1310.91 AC16 VSS 4655.5 1310.91 AC18 VSS 4655.5 1310.91 AC19 VSS 4655.5 1310.91 AC2 VCCPRIM_3P3 9038.59 1288.29 AC21 VSS 3864.9 1310.91 AC24 VCCIO 2369.6 1310.91 AC24 VCCIO 2379 1310.91 AC27 VSS 1883.7 1310.91 AC27 VSS 1883.7 1310.91 AC26 VCCIO 2379 1310.91 AC27 VSS 1883.7 1310.91 AC29 VCCSA 893.1 1310.91 AC23 VCC 937.8 1310.91 AC30 VCSA 937.8 1310.91 <	AB64	VCCGT				-9310.37	-1610.36	
AB9 GPP_C18 / 12C1_SDA 7313.93 1610.36 AC10 GPP_C4 / SNLDDATA 7667.55 1288.29 AC12 GP_C0 / SMBCLK 6574.79 1288.29 AC15 VSS 550.8 1310.91 AC16 VSS 4655.5 1310.91 AC18 VSS 4655.5 1310.91 AC19 VSS 4655.5 1310.91 AC2 VCCPRIM_3P3 9038.59 1288.29 AC21 VSS 3864.9 1310.91 AC24 VCCIO 2369.6 1310.91 AC24 VCCIO 2379 1310.91 AC27 VSS 1883.7 1310.91 AC27 VSS 1883.7 1310.91 AC26 VCCIO 2379 1310.91 AC27 VSS 1883.7 1310.91 AC29 VCCSA 893.1 1310.91 AC23 VCC 937.8 1310.91 AC30 VCSA 937.8 1310.91 <	4 87	GPP_C14 / UART1_RTS# /		de		7806.69	-1610.36	sine
AC10 GPP_C4 / SML0DATA 7067.55 1288.29 AC12 GPP_C0 / SMBCLK 6574.79 1288.29 AC16 VSS 3360.8 1310.91 AC16 VSS 3360.8 1310.91 AC18 VSS 4350.2 1310.91 AC19 VSS 4360.2 1310.91 AC19 VSS 4360.2 1310.91 AC21 VSS 364.9 1310.91 AC22 VCCIO 386.4.9 1310.91 AC24 VCCIO 2874.3 1310.91 AC24 VCCIO 2874.3 1310.91 AC24 VCSS 188.37 1310.91 AC24 VCSA 1388.4 1310.91 AC20 VCSA 993.1 1310.91 AC21 VSS 97.8 1310.91 AC30 VCSA 893.1 1310.91 AC32 VCC 97.8 1310.91 AC33 VSS 97.5 1310.91				June		7212.02	1610.26 1	
AC12 GPP_C0 / SMBCLK 6574.79 1288.29 AC15 VSS SS S36.6.1 1310.91 AC16 VSS 485.5.5 1310.91 AC18 VSS 485.5.5 1310.91 AC19 VSS 485.5.5 1310.91 AC2 VCCPRIM_3P3 9038.59 1288.29 AC21 VSS 3864.9 1310.91 AC2 VCCRIM_3P3 9038.59 1288.29 AC21 VSS 3864.9 1310.91 AC22 VCCIO 2874.3 1310.91 AC24 VCCIO 1883.7 1310.91 AC26 VCCSTG 1883.7 1310.91 AC27 VCSA 1883.4 1310.91 AC32 VCCA 997.8 1310.91 AC32 VCCGA 997.8 1310.91 AC33 VSS 191.91 130.91 AC34 VCCGA 997.8 1310.91 AC35 VCCG0 97.5 1310.91<				Aineu				
AC15 VSS Image: state				Ser.			5	
AC16 VSS 1310.91 AC18 VSS 4855.5 1310.91 AC19 VSS 4855.5 1310.91 AC2 VCCPRIM_3P3 9038.59 1288.29 AC21 VSS 3364.9 1310.91 AC22 VCSPRIM_3P3 200 3364.9 1310.91 AC23 VCCI0 2874.3 1310.91 AC24 VCCI0 2874.3 1310.91 AC26 VCCSTG 2874.3 1310.91 AC27 VSS 288.4 1310.91 AC26 VCCSTG 2379 4310.91 AC27 VSS 2874.3 1310.91 AC28 VCCSA 1888.4 1310.91 AC29 VCSA 937.8 1310.91 AC30 VCSA 937.8 1310.91 AC30 VCSA 97.5 1310.91 AC30 VS5 108.11 1310.91 AC30 VS5 2076.7 130.91 AC40<			d U					
AC18 VSS 4855.5 -1310.91 AC19 VSS 4360.2 -1310.91 AC2 VCCPRIM_3P3 9038.59 -1288.29 AC21 VSS 3864.9 -1310.91 AC2 VCCIO 3369.6 -1310.91 AC23 VCCIO 2874.3 -1310.91 AC24 VCCIO 2874.3 -1310.91 AC25 VCCSTG 2379 -1310.91 AC26 VCCSA 1883.7 -1310.91 AC29 VCCSA 97.8 -1310.91 AC30 VCCSA 893.1 -1310.91 AC30 VCCSA 97.5 -1310.91 AC33 VSS - -97.5 -1310.91 AC33 VSS - -97.5 -1310.91 AC34 VCCG0 - -97.5 -1310.91 AC35 VCCG0 - -97.5 -1310.91 AC44 VCCG0 - -97.5 -1310.91 AC40 </td <td></td> <td></td> <td>i cfine</td> <td></td> <td></td> <td>0</td> <td></td> <td></td>			i cfine			0		
AC19 VSS 4360.2 -1310.91 AC2 VCCPRIM_3P3 9038.59 -1288.29 AC21 VSS 3864.9 -1310.91 AC23 VCCIO 3369.6 -1310.91 AC24 VCCIO 3369.6 -1310.91 AC25 VCCIO 2874.3 -1310.91 AC26 VCCTO 2879.3 -1310.91 AC27 VSS 2379 -1310.91 AC26 VCCSTG 2379 -1310.91 AC27 VSS 1883.7 -1310.91 AC28 VCCSA 1388.4 -1310.91 AC30 VCCSA 993.1 -1310.91 AC31 VSS -97.5 -1310.91 AC33 VSS -97.5 -1310.91 AC34 VSS -97.5 -1310.91 AC35 VCC60 -992.8 -1310.91 AC46 VSS -97.57 -1310.91 AC43 VSC -97.57 -1310.91	- U*		Inde		illion and a second			
AC2 VCCPRIM_3P3 9038.59 -1288.29 AC21 VSS 3664.9 -1310.91 AC23 VCCIO 3369.6 -1310.91 AC24 VCCIO 2874.3 -1310.91 AC24 VCCIO 2379 -1310.91 AC24 VCCIG 2379 -1310.91 AC25 VCSS 1883.7 -1310.91 AC26 VCCSA 1883.7 -1310.91 AC30 VCCSA 893.1 -1310.91 AC32 VCC 397.8 -1310.91 AC33 VSS 97.5 -1310.91 AC33 VCCG0 -97.5 -1310.91 AC34 VCCG0 -97.8 -1310.91 AC35 VCCG0 -97.8 -1310.91 AC36 VSS -1088.1 -1310.91 AC30 VCSG0 -1583.4 -1310.91 AC40 VSS -278.7 -1310.91 AC41 VCCGT -278.4 -1310.91 <t< td=""><td></td><td></td><td>Y.</td><td></td><td>2 un</td><td></td><td></td><td></td></t<>			Y.		2 un			
AC21 VSS 3864.9 -1310.91 AC23 VCCIO 3369.6 -1310.91 AC24 VCCIO 2874.3 -1310.91 AC26 VCCSTG 2874.3 -1310.91 AC27 VSS 1883.7 -1310.91 AC28 VCCSA 1388.4 -1310.91 AC30 VCCSA 393.1 -1310.91 AC30 VCCSA 997.8 -1310.91 AC31 VSS -97.5 -1310.91 AC33 VSS -97.5 -1310.91 AC35 VCCG0 -97.5 -1310.91 AC36 VSS -97.5 -1310.91 AC38 VCCG0 -1088.1 -1310.91 AC38 VCCG0 -1088.1 -1310.91 AC4 GPC_13 / UART1_TXD / ISH_UART1_TXD 8454.83 1288.29 AC40 VSS -2078.7 -1310.91 AC41 VCCGT -2078.7 -1310.91 AC43 VCCGT -3069.3					sine"			
AC23 VCCIO 3369.6 1310.91 AC24 VCCIO 2874.3 1310.91 AC26 VCCSTG 2379 1310.91 AC27 VSS 1883.7 1310.91 AC29 VCCSA 1883.7 1310.91 AC29 VCCSA 1883.7 1310.91 AC30 VCCSA 97.8 1310.91 AC31 VSS 97.8 1310.91 AC32 VCC 97.5 1310.91 AC33 VCCG0 97.5 1310.91 AC34 VCSS 97.5 1310.91 AC35 VCCG0 97.5 1310.91 AC36 VSS 100.1 198.1 AC40 VSS 1310.91 1310.91 AC41 VCCG 207.8 1310.91 AC41 VCCG 207.8 1310.91 AC41 VCCG 90.91 1310.91 AC44 VCCGT 207.8 1310.91 AC44				Ó	81.			SUU
AC26 VCCSTG 2379 4310.91 AC27 VSS 1883.7 -1310.91 AC29 VCCSA 1388.4 -1310.91 AC30 VCCSA 893.1 -1310.91 AC32 VCC 397.8 -1310.91 AC32 VCC 997.8 -1310.91 AC33 VSS - -97.5 -1310.91 AC35 VCCG0 -97.5 -1310.91 AC36 VSS - -97.5 -1310.91 AC36 VSS - -97.5 -1310.91 AC36 VSS - -1088.1 -1310.91 AC40 VSS - -1088.1 -1310.91 AC41 VCC - -2078.7 -1310.91 AC42 VCGT - -3069.3 -1310.91 AC44 VCCGT - -3069.3 -1310.91 AC44 VCGT - -3069.3 -1310.91 AC44 VCGT -		20		od Uli		3369.6		
AC27 VSS 1883.7 -1310.91 AC29 VCCSA 1388.4 -1310.91 AC30 VCCSA 893.1 -1310.91 AC32 VCC 397.8 -1310.91 AC33 VSS 97.5 -1310.91 AC35 VCCG0 97.5 -1310.91 AC36 VSS 97.5 -1310.91 AC40 VSS 97.5 -1310.91 AC41 VCCG0 97.5 -1310.91 AC42 VCGGT 2078.7 -1310.91 AC43 VCCGT 90.00 -2078.7 -1310.91 AC44 VCCGT 90.00 -3564.6 -1310.91 AC44 VCCGT 90.00 -3564.6 -1310.91 AC44 VCCGT 90.00 -3564.6 -1310.91 AC44 VCCGT 90.00	AC24	VCCIO		1 of ine		2874.3	-1310.91	
AC29 VCCSA 1388.4 -1310.91 AC30 VCCSA 893.1 -1310.91 AC32 VCC 397.8 -1310.91 AC33 VSS 97.5 -1310.91 AC33 VSS 97.5 -1310.91 AC35 VCCG0 97.5 -1310.91 AC36 VSS -1088.1 -1310.91 AC36 VSS -1088.1 -1310.91 AC36 VSS -1088.1 -1310.91 AC4 GPP_C13 / UART1_TXD / ISH_UART1_TXD 8545.83 -1288.29 AC40 VSS -2078.7 -1310.91 AC41 VCC -2574 -1310.91 AC43 VCCGT -2574 -1310.91 AC44 VCCGT -2574 -1310.91 AC44 VCCGT -2574 -1310.91 AC44 VCCGT -2574 -1310.91 AC44 VCCGT -3564.6 -1310.91 AC47 VCCGT -5555.2 -1310.91 AC49 VCGT -5605.5 -1310.91		VCCSTG		MOB		2379	-1310.91	
AC30 VCCSA 893.1 -1310.91 AC32 VCC 397.8 -1310.91 AC33 VSS -97.5 -1310.91 AC35 VCCG0 -97.5 -1310.91 AC36 VSS -1088.1 -1310.91 AC36 VSS -1088.1 -1310.91 AC36 VSS -1088.1 -1310.91 AC4 GPP_C13 / UART1_TXD / ISH_UART1_TXD 8545.83 -1288.29 AC40 VSS -2078.7 -1310.91 AC41 VCC -2078.7 -1310.91 AC42 VCGT -2078.7 -1310.91 AC44 VCCGT -2078.7 -1310.91 AC45 VCCGT -2055.5 -1310.91 AC46 VCCGT -5555.5 -1310.91 <	AC27	VSS	ed			1883.7	-1310.91	
AC32 VCC 397.8 -1310.91 AC33 VSS -97.5 1310.91 AC35 VCCG0 -97.5 1310.91 AC36 VSS -1088.1 1310.91 AC36 VSS -1088.1 1310.91 AC36 VSS -1088.1 1310.91 AC37 VCCG0 -1583.4 1310.91 AC4 GPP_C13 / UART1_TXD / ISH_UART1_TXD 8545.83 1288.29 AC40 VSS -2078.7 1310.91 AC41 VCC -2076.7 1310.91 AC43 VCCGT -3069.3 1310.91 AC44 VCCGT -3069.3 1310.91 AC44 VCCGT -3069.3 1310.91 AC44 VCCGT -4059.9 1310.91 AC45 VCCGT -4059.9 1310.91 AC46 VCCGT -556.5 1310.91 AC47 VCCGT -5550.5 1310.91 AC49 VCCGT -5545.8 1310.91 AC50 VCCGT -6041.1 1310.91	AC29	VCCSA	ACTIN		é.	1388.4	-1310.91	
AC33 VSS 97.5 -1310.91 AC35 VCCG0 97.5 -1310.91 AC36 VSS 108.1 -1088.1 -1310.91 AC36 VSS 108.1 -1088.1 -1310.91 AC38 VCCG0 1088.1 -1088.1 -1310.91 AC4 GPP_C13/UART1_TXD / ISH_UART1_TXD 8545.83 -1288.29 AC40 VSS 2078.7 -1310.91 AC41 VCC 22774 -1310.91 AC43 VCCGT 2078.7 -1310.91 AC44 VCCGT 3069.3 -1310.91 AC44 VCCGT 3069.3 -1310.91 AC44 VCCGT -3564.6 -1310.91 AC45 VCCGT -4059.9 -1310.91 AC46 VCCGT -4055.2 -1310.91 AC47 VCCGT -5050.5 1310.91 AC49 VCCGT -5050.5 1310.91 AC50 VCCGT -5051.9 -5051.91 AC51 VCCGT -6041.1 1310.91 AC53 VCC	AC30	VCCSA	Uno		nde'	893.1	-1310.91	
AC35 VCCG0 -592.8 -1310.91 AC36 VSS -1088.1 -1310.91 AC38 VCCG0 -1583.4 -1310.91 AC4 GPP_C13 / UART1_TXD / ISH_UART1_TXD 8545.83 -1288.29 AC40 VSS - - 2078.7 -1310.91 AC41 VCC - - -2078.7 -1310.91 AC43 VCCGT - - -2078.7 -1310.91 AC44 VCCGT - - -2078.7 -1310.91 AC44 VCCGT - - -2078.7 -1310.91 AC44 VCCGT - - -3069.3 -1310.91 AC45 VCCGT - - -3564.6 -1310.91 AC46 VCCGT - - -4059.9 -1310.91 AC47 VCCGT - - -555.5 -1310.91 AC50 VCGT - - -5545.8 -1310.91 AC51 VCGT - - -5545.8 -1310.91 AC52 <t< td=""><td>AC32</td><td>VCC</td><td></td><td></td><td>d y</td><td>397.8</td><td>-1310.91</td><td></td></t<>	AC32	VCC			d y	397.8	-1310.91	
AC36 VSS -1088.1 -1310.91 AC38 VCCG0 -1583.4 -1310.91 AC4 GPP_C13 / UART1_TXD / ISH_UART1_TXD 8545.83 -1288.29 AC40 VSS -2078.7 -1310.91 AC41 VCC -2574 -1310.91 AC43 VCCGT -2678.7 -1310.91 AC44 VCCGT -2674 -1310.91 AC44 VCCGT -2674 -1310.91 AC45 VCCGT -2678.7 -1310.91 AC46 VCCGT -3069.3 -1310.91 AC47 VCCGT -2574 -1310.91 AC47 VCCGT -4555.2 -1310.91 AC49 VCCGT -4555.2 -1310.91 AC50 VCCGT -2545.8 1310.91 AC51 VCCGT -6041.1 -1310.91 AC53 VCCGT -6041.1 -1310.91 AC53 VCCGT -6041.1 -1310.91 AC55 VCCGT -6041.1 -1310.91 AC55 VCCGT -6041.1 -1310.91 <td>AC33</td> <td>VSS</td> <td></td> <td></td> <td>atine</td> <td>-97.5</td> <td>-1310.91</td> <td></td>	AC33	VSS			atine	-97.5	-1310.91	
AC38 VCCG0 -1583.4 -1310.91 AC4 GPP_C13 / UART1_TXD / ISH_UART1_TXD 8545.83 -1288.29 AC40 VSS -2078.7 -1310.91 AC41 VCC -2574 -1310.91 AC43 VCCGT -2574 -1310.91 AC44 VCCGT -3069.3 -1310.91 AC45 VCCGT -3564.6 -1310.91 AC46 VCCGT -4059.9 -1310.91 AC47 VCCGT -4059.9 -1310.91 AC49 VCCGT -4555.2 -1310.91 AC49 VCCGT -5050.5 -1310.91 AC50 VCCGT -5545.8 -1310.91 AC51 VCCGT -6041.1 -1310.91 AC52 VCCGT -6041.1 -1310.91 AC53 VCCGT -6041.1 -1310.91 AC53 VCCGT -6041.1 -1310.91 AC54 VCCGT -6041.1 -1310.91 AC55 VCCGT -6041.1 -1310.91 AC55 VCCGT -6041.1 -130	AC35	VCCG0		10	20	-592.8	-1310.91	
AC4 GPP_C13 / UART1_TXD / ISH_UART1_TXD 8545.83 +1288.29 AC40 VSS -2078.7 +1310.91 AC41 VCC -2574 -1310.91 AC43 VCCGT -3069.3 +1310.91 AC44 VCCGT -3564.6 +1310.91 AC46 VCCGT -4059.9 +1310.91 AC47 VCCGT -4555.2 +1310.91 AC49 VCCGT -4555.2 +1310.91 AC49 VCCGT -5050.5 +1310.91 AC50 VCCGT -6041.1 +1310.91 AC51 VCCGT -6574.79 +1288.29 AC55 VCCGT -6574.79 +1288.29 AC55 VCCGT -6574.79 +1288.29 AC55 VCCGT -6574.79 +1288.29 AC56 VCCGT -7067.55 +1288.29 AC57 VCCGT -7067.55 +1288.29 AC59 VCCGT -7067.55 +1288.29 AC59 VCCGT -8053.07 +1288.29 AC59 VCCGT -8053.07	AC36	vss		ed		-1088.1	-1310.91	
AC40 VSS -2078.7 -1310.91 AC41 VCC -2574 -1310.91 AC43 VCCGT -3069.3 -1310.91 AC44 VCCGT -3564.6 -1310.91 AC46 VCCGT -4059.9 -1310.91 AC47 VCCGT -4059.9 -1310.91 AC49 VCCGT -4059.9 -1310.91 AC49 VCCGT -4059.9 -1310.91 AC49 VCCGT -4059.9 -1310.91 AC50 VCCGT -5050.5 -1310.91 AC51 VCCGT -6041.1 -1310.91 AC53 VCCGT -6574.79 -1288.29 AC55 VCCGT -7067.55 -1288.29 AC55 VCCGT -7560.31 -1288.29 AC59 VCCGT -7560.31 -1288.29 AC59 VCCGT -8053.07 -1288.29 AC59 VCCGT -7560.31 -1288.29 AC59 VCCGT -8053.07 -1288.29 AC59 VCCGT -7560.31 -1288.29	AC38	VCCG0		16 mil		-1583.4	-1310.91	
AC41 VCC -2574 -1310.91 AC43 VCCGT -3069.3 -1310.91 AC44 VCCGT -3564.6 -1310.91 AC44 VCCGT -4059.9 -1310.91 AC46 VCCGT -4059.9 -1310.91 AC47 VCCGT -4059.9 -1310.91 AC49 VCCGT -4555.2 -1310.91 AC50 VCCGT -5545.8 -1310.91 AC51 VCCGT -6041.1 -1310.91 AC53 VCCGT -6041.1 -1310.91 AC55 VCCGT -6041.1 -1310.91 AC55 VCCGT -6041.1 -1310.91 AC55 VCCGT -6041.1 -1310.91 AC50 VCCGT -6041.1 -1310.91 AC55 VCCGT -6041.1 -1310.91 AC55 VCCGT -6041.1 -1310.91 AC55 VCCGT -6041.1 -1310.91 AC55 VCCGT -7067.55 -1288.29 AC57 VCCGT -7560.31 -1288.29	AC4	GPP_C13 / UART1_TXD / ISH_UART1_TXD	2	MAG		8545.83	-1288.29	
AC43 VCCGT -3069.3 -1310.91 AC44 VCCGT -3564.6 -1310.91 AC46 VCCGT -4059.9 -1310.91 AC47 VCCGT -4555.2 -1310.91 AC49 VCCGT -4555.2 -1310.91 AC50 VCCGT -5545.8 -1310.91 AC51 VCCGT -5545.8 -1310.91 AC53 VCCGT -6041.1 -1310.91 AC53 VCCGT -6041.1 -1310.91 AC55 VCCGT -6041.1 -1310.91 AC55 VCCGT -6041.1 -1310.91 AC50 VCCGT -6041.1 -1310.91 AC51 VCCGT -6041.1 -1310.91 AC55 VCCGT -7067.55 -1288.29 AC55 VCCGT -7067.55 -1288.29 AC59 VCCGT -8053.07 -1288.29 AC6 GPP_C12 / UART1_RXD / ISH_UART1_RXD 8053.07 -1288.29		767	cineo			-2078.7		
AC44 VCCGT -3564.6 -1310.91 AC46 VCCGT -4059.9 -1310.91 AC47 VCCGT -4555.2 -1310.91 AC49 VCCGT -4555.2 -1310.91 AC50 VCCGT -5050.5 -1310.91 AC51 VCCGT -5050.5 -1310.91 AC53 VCCGT -6041.1 -1310.91 AC53 VCCGT -6041.1 -1310.91 AC53 VCCGT -6041.1 -1310.91 AC54 VCCGT -6041.1 -1310.91 AC55 VCCGT -6041.1 -1310.91 AC55 VCCGT -6041.1 -1310.91 AC55 VCCGT -6041.1 -1310.91 AC55 VCCGT -6074.79 -1288.29 AC55 VCCGT -7067.55 -1288.29 AC59 VCCGT -8053.07 -1288.29 AC6 GPP_C12 / UART1_RXD / ISH_UART1_RXD 8053.07 -1288.29	AC41	VCC	der			-2574	-1310.91	
AC49 VCCGT 5050.5 1510.51 AC50 VCCGT -5545.8 -1310.91 AC51 VCCGT -6041.1 -1310.91 AC53 VCCGT -6574.79 -1288.29 AC55 VCCGT -7067.55 -1288.29 AC57 VCCGT -7560.31 -1288.29 AC59 VCCGT -8053.07 -1288.29 AC6 GPP_C12 / UART1_RXD / ISH_UART1_RXD 8053.07 -1288.29			JUIN		inde			
AC49 VCCGT 5050.5 1510.51 AC50 VCCGT -5545.8 -1310.91 AC51 VCCGT -6041.1 -1310.91 AC53 VCCGT -6574.79 -1288.29 AC55 VCCGT -7067.55 -1288.29 AC57 VCCGT -7560.31 -1288.29 AC59 VCCGT -8053.07 -1288.29 AC6 GPP_C12 / UART1_RXD / ISH_UART1_RXD 8053.07 -1288.29			-		ed		-1310.91	
AC49 VCCGT 5050.5 1510.51 AC50 VCCGT -5545.8 -1310.91 AC51 VCCGT -6041.1 -1310.91 AC53 VCCGT -6574.79 -1288.29 AC55 VCCGT -7067.55 -1288.29 AC57 VCCGT -7560.31 -1288.29 AC59 VCCGT -8053.07 -1288.29 AC6 GPP_C12 / UART1_RXD / ISH_UART1_RXD 8053.07 -1288.29					1eril 1		-1310.91	<u>c</u> \
AC49 VCCGT 5050.5 1510.51 AC50 VCCGT -5545.8 -1310.91 AC51 VCCGT -6041.1 -1310.91 AC53 VCCGT -6574.79 -1288.29 AC55 VCCGT -7067.55 -1288.29 AC57 VCCGT -7560.31 -1288.29 AC59 VCCGT -8053.07 -1288.29 AC6 GPP_C12 / UART1_RXD / ISH_UART1_RXD 8053.07 -1288.29				10 -	м. Г		-1310.91	ndefi
AC51 VCCGT -6041.1 -1310.91 AC53 VCCGT -6574.79 -1288.29 AC55 VCCGT -7067.55 -1288.29 AC57 VCCGT -7560.31 -1288.29 AC59 VCCGT -8053.07 -1288.29 AC6 GPP_C12 / UART1_RXD / ISH_UART1_RXD 8053.07 -1288.29				en eo			1510.51	
AC53 VCCGT -6574.79 -1288.29 AC55 VCCGT -7067.55 -1288.29 AC57 VCCGT -7560.31 -1288.29 AC59 VCCGT -8053.07 -1288.29 AC6 GPP_C12 / UART1_RXD / ISH_UART1_RXD 8053.07 -1288.29				den			511.	
AC55 VCCGT -7067.55 -1288.29 AC57 VCCGT -7560.31 -1288.29 AC59 VCCGT -8053.07 -1288.29 AC6 GPP_C12 / UART1_RXD / ISH_UART1_RXD 8053.07 -1288.29				UI.				
AC57 VCCGT -7560.31 -1288.29 AC59 VCCGT -8053.07 -1288.29 AC6 GPP_C12 / UART1_RXD / ISH_UART1_RXD 8053.07 -1288.29		26M	sine'			0		
AC59 VCCGT -8053.07 -1288.29 AC6 GPP_C12 / UART1_RXD / ISH_UART1_RXD 8053.07 -1288.29			de.).			
AC6 GPP_C12 / UART1_RXD / ISH_UART1_RXD 8053.07 -1288.29			<u>d V'</u>		1 uno			
AC61 VCCGT -8545.83 -1288.29 Datasheet, Volume 1 of 2 181	9				0.90		-1288 20	
Datasheet, Volume 1 of 2 181					berr.		-1288 29	
unde. define		Datasheet, Volume 1 of 2		d undefined u	1.		undefined V	Inor
		unde	undefill			Jefineu		

	(intel) and undefine		-96	stine		4011	ner
	(intal) red		ned une	U-Quad Core/YProd	ressor Ball	inc	
	(inter		defille			sinegon	
		1	nuc.			Je.	
	Table 9-2. Y-Processor Ball	List (Sheet 4	of 40)		ned un		
Ball #	Ball Name	UN LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]	
AC63	VCCGT			aneo	-9038.59	-1288.29	
AC8	GPP_C8 / UART0_RXD		5-	e	7560.31	-1288.29	in.
AD1	VCCPRIM_3P3		d un		9310.37	-966.22	
AD11	GPP_C16 / I2C0_SDA		sin ^{ou}		6821.17	-966.22	
AD13	VSS		vge,		6328.41	-961.14	
AD3	GPP_C22 / UART2_RTS#	6-			8792.21	-966.22	
AD5	GPP_C20 / UART2_RXD	AINE			8299.45	-966.22	
AD54	VCCGT	nde		10	-6821.17	-966.22	
AD56	VCCGT	0		, una-	-7313.93	-966.22	
AD58	VCCGT			ed -	-7806.69	-966.22	
AD60	VCCGT			Ye	-8299.45	-966.22	
AD62	VCCGT		- UP		-8792.21	-966.22	5
AD64	VCCGT		^{CO} 90ia		-9310.37	-966.22	
AD7	GPP_C21 / UART2_TXD		delli		7806.69	-966.22	
	GPP_C23 / UART2_CTS#	2			7313.93	-966.22	
	VSS	sine'			7067.55	-644.14	
AE12	GPP_G7 / SD_WP	nder		20	6574.79	-644.14	
	VCCATS	0.		ino.	5846.1	-752.11	
	VCCATS			ed	5350.8	-752.11	
	VCCPRIM_CORE			76,11,-	4855.5	-752.11	
	VCCPRIM_CORE		, v		4360.2	-752.11	,e,
	VSS		090		9038.59	-644.14	
	VSS		dein.		3864.9	-752.11	
	VCCIO		d un		3369.6	-752.11	
	VCCIO	97112	C.		2874.3	-752.11	
	VCCIO	ole''			2379	-752.11	
0	VCCPLL_OC	d'un.		in ^o	1883.7		
	VCCSA			ed	1388.4	-752.11	
	VSS			76 <u>11</u> 1	893.1	-752.11	
	VCC			<u> </u>	397.8	-752.11 -752.11 -752.11 -752.11	9e
	VCC		fined		-97.5	-752.11	
	VCC		dern		-592.8	-752.11	
	VCC		A UNIT		-1088.1	-752.11	
	VCC	772	er		-1583.4	-752.11	
	VSS	nde'''			8545.83	-644.14	
	VCC	d'h.		77.	-2078.7	-752.11	
	VCC			ed v	-2574	-752.11	
	VSS			4111-	-3069.3	-752.11	
ΔF44	VSS			unos	-3564.6	-752.11	.0
<u> </u>	182 182 undefined undefine	14	ned undefined	1	Datasheet, V	-752.11 -752.11 -752.11 Volume 1 of 2	Ъ. ⁻
	dunt	d under.			ndefine		



Table 9-2.

	undefine		def	ineo			efined
	U/U-Quad Core/YProcessor BallInfor	mation	defined une		(ir	itel	9e.
6	Table 9-2. Y-Processor Ball	LList (Sheet 5	of 40)		ed une		
Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]	
AE46	VSS			ed	-4059.9	-752.11	
AE47	VSS		20		-4555.2	-752.11	
AE49	VSS		4 UNC		-5050.5	-752.11	
AE50	VSS		cin ^{eo}		-5545.8	-752.11	
AE51	VSS		delli		-6041.1	-752.11	
AE53	VCCGT	- 24	P		-6574.79	-644.14	
AE55	VCCGT	since			-7067.55	-644.14	
AE57	VCCGT	nde'		16/11	-7560.31	-644.14	
AE59	VCCGT	Ó.		, uno	-8053.07	-644.14	
AE6	USB2_VBUSSENSE			ed	8053.07	-644.14	
AE61	VCCGT			e	-8545.83	-644.14	
AE63	VCCGT		4 UNC		-9038.59	-644.14	nder.
AE8	VSS		sineu		7560.31	-644.14	
AF1	VCCPGPPD		gej,		9310.37	-322.07	
AF11	GPP_G4 / SD_DATA3	-6	0		6821.17	-322.07	
AF13	VSS	finec			6328.41	-316.99	
AF15	VSS			192	5846.1	-193.31	
AF16	VSS	20		, uno-	5350.8	-193.31	
AF18	VCCPRIM_CORE	5		ea	4855.5	-193.31	
AF19	VCCPRIM_CORE			e	4360.2	-193.31	
AF21	VSS		d un	Y	3864.9	-193.31	uger.
AF23	VSS		sineu		3369.6	-193.31	
AF24	VCCIO		dell		2874.3	-193.31	
AF26	VCCIO	6			2379	-193.31	
AF27	VCCPLL_OC	Aines			1883.7	-193.31	
AF29	VCCSA	ndei		26	1388.4	-193.31	
AF3	USB2P_7	e0 11		, uno-	8792.21	-322.07	
AF30	VCCSA			the contract of the contract o	893.1	-193.31	
AF32	vcc			deith	397.8	-193.31	
AF33	vss		AUT		-97.5	-193.31	undefil
AF35	VCCG1		^U ON <i>i</i> a		-592.8	-193.31	, v.
AF36	vss		ndei		-1088.1	-193.31	
AF38	VCCG1		0		-1583.4	-193.31	
AF40	VSS	fine			-2078.7	-193.31	
AF41	vcc	, nde		X	-2574	-193.31	
AF43	VCCGT	ed vi			-3069.3	-193.31	
AF44	VCCGT	ll.		^O 9nis	-3564.6	-193.31	
AF46	VCCGT			detill	-4059.9	-193.31	
AF47	VCCGT		20		-4555.2	-193.31	
	Datasheet, Volume 1 of 2	nis	ed undefined u		6	undefine 183	d undefi
	undefill	ed under.		inc	efine		



Table 9-2.

	(intel) red undefine		-96	stin		Acti	'Ue
	red		ed une			inc	
			lefine 0/	U-Quad Core/YProc	cessor Ball	Information	
			noc			Jeffi	
	- ALIA	ined i			dun		
n,	Table 9-2. Y-Processor Ball I	List (Sheet 6 o	f 40)		Uer.		
Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]	
AF49	VCCGT				-5050.5	-193.31	
	USB2N_7		2	C	8299.45	-322.07	n_{i}
	VCCGT		, une	2	-5545.8	-193.31	
	VCCGT		Contraction of the second		-6041.1	-193.31	
-	VSS		deilli		-6821.17	-322.07	
	VSS		300		-7313.93		
	VSS	sineu			-7806.69	-322.07	
	VSS	ndel.		0	-8299.45		
20	VSS			inde	-8792.21	-322.07	
-	VSS			ed v	-9310.37	-322.07	
	USB2_ID			4611-	7806.69	-322.07	
	GPP_G3 / SD_DATA2		ຸ ມາ		7313.93	-322.07	31.
	GPP_G6 / SD_CLK		Contra A		7067.55		
	GPP_G2 / SD_DATA1		dein		6574.79	0	
	VCCPGPPD	2	din -		9038.59	0	
	USB2P_9	sine ^o			8545.83	0	
	VCCGT	ndel.		10	-6574.79	0	
~0	DDR1_DQ[14] / DDR0_DQ[30]	-0- -11.	DDR1_DQ[14]	DDR0_DQ[30]	-7067.55		
	DDR1_DQ[15] / DDR0_DQ[31]	4°	DDR1_DQ[15]	DDR0_DQ[31]	-7560.31		
	VSS			26111			
	USB2N_9		1	0	8053.07	0	
AG61	DDR0_DQ[0]		O9nia		-8545.83	0 0	
	DDR0_DQ[5]		dein.		-9038.59	0	
AG8	GPP_G5 / SD_CD#		U.I.		7560.31	0	
AH1	VCCPGPPC	-fine			9310.37	322.07	
AH11	GPP_G1 / SD_DATA0			2	6821.17	322.07	
AH13	VCCPRIM_1P0	ed W		, uno	6328.41	327.15	
AH15	VCCPRIM_1P0	1		aned.	5846.1	365.49	
AH16	VSS	1		den	5350.8	327.15 365.49 365.49 365.49	
AH18	VCCPRIM_1P0	1	14	N.C.	4855.5	365.49	'9 ₆
AH19	VCCPRIM_1P0		fineo		4360.2	365.49	
AH21	VCCPRIM_3P3		ndei		3864.9	365.49	
AH23	VSS		0.00		3369.6	365.49	
AH24	VSS	nine -			2874.3	365.49	
AH26	VCCIO	inde			2379	365.49	
AH27	VSS	edu		<u>_ un</u>	1883.7	365.49	
AH29	VCCSA			⁰ 9nis	1388.4	365.49	
AH3	USB2P_5	1		deit	8792.21	322.07	
AH30	VSS		2	Un	893.1	365.49	
	184 undefined undefine	13	ed undefined	ſ	Datasheet, Y	365.49 322.07 365.49 Volume 1 of 2	
	dutte	a unde.			defille		



	undefine		def	ineo			stined
	U/U-Quad Core/YProcessor BallInform	ation	defined unc		(ir	ntel	
2	etined	ined un			d une		
duno	Table 9-2. Y-Processor Ball I	<u>nou</u>		Non-Interleaved	6-		
Ball #	Ball Name	LPDDR3	Interleaved (IL)	(NIL)	X [um]	Y [um]	
AH32	VCC			sine	397.8	365.49	
AH33	vss		nde		-97.5	365.49	stine
AH35	VCCG1		d'un		-592.8	365.49	
AH36	VSS		sine		-1088.1	365.49	
AH38	VCCG1		nde.		-1583.4	365.49	
AH40	VSS	ed v			-2078.7	365.49	
AH41	VCC	1efin-			-2574	365.49	
AH43	VSS	Inos		den	-3069.3	365.49	
AH44	vss			dun	-3564.6	365.49	
AH46	VSS			sinet	-4059.9	365.49	
AH47	vss		6	e.	-4555.2	365.49	stine
AH49	VSS		dui		-5050.5	365.49	
AH5	USB2N_5		sine		8299.45	322.07	
AH50	VSS		Nge.		-5545.8	365.49	
AH51	VSS	6	0		-6041.1	365.49	
AH54	VSS	efine			-6821.17	322.07	
AH56	DDR1_DQ[11] / DDR0_DQ[27]	INOS	DDR1_DQ[11]	DDR0_DQ[27]	-7313.93	322.07	
AH58	DDR1_DQ[10] / DDR0_DQ[26]		DDR1_DQ[10]	DDR0_DQ[26]	-7806.69	322.07	
AH60	DDR0_DQ[1]			cineo.	-8299.45	322.07	
AH62	DDR0_DQ[4]			Jerri	-8792.21	322.07	nip.
AH64	VDDQ		dur		-9310.37	322.07	nde
AH7	RSVD		sines		7806.69	322.07	
AH9	GPP_G0 / SD_CMD		nde.		7313.93	322.07	
AJ10	GPP_F16 / EMMC_DATA3	6			7067.55	644.14	
AJ12	GPP_F19 / EMMC_DATA6	fine			6574.79	644.14	
AJ2	VCCPGPPC	nde		26	9038.59	644.14	
AJ4	USB2P_1	þ.		, une	8545.83	644.14	
AJ53	VCCGT	/		aneo.	-6574.79	644.14	
AJ55	DDR1_DQSP[1] / DDR0_DQSP[3]		DDR1_DQSP[1]	DDR0_DQSP[3]	-7067.55	644.14	
AJ57	DDR1_DQSN[1] / DDR0_DQSN[3]		DDR1_DQSN[1]	DDR0_DQSN[3]	-7560.31	644.14	undefil
AJ59	VSS		sines		-8053.07	644.14	
AJ6	USB2N_1		nde.		8053.07	644.14	
AJ61	DDR0_DQSN[0]		200		-8545.83	644.14	
AJ63	DDR0_DQSP[0]	fine	-		-9038.59	644.14	
AJ8	GPP_F23	inde.			7560.31	644.14	
AK1	VSS	<u>d</u>		, uno	9310.37	966.22	
AK11	vss			Anea	6821.17	966.22	
AK13	VSS			defili	6328.41	971.3	
AK15	VSS		20		5846.1	924.29	
	Datasheet, Volume 1 of 2	inis	ad undefined t		6	966.22 966.22 971.3 924.29 185	
	undefine	od under.		inc	lefine		



Table 9-2.

	thed undefine			SUI.		in	<i>ve</i>
	(intel)		ed un		- "	- unde	
			lefine U/	U-Quad Core/YPro	cessor Ball	Information	
			Inoc			etti	
	etine	ed t			dun		
n, .	Table 9-2. Y-Processor Ball I	List (Sheet 8 o	of 40)	13	nec		
Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]	
AK16	VSS			ed	5350.8	924.29	
	VCCPRIM_1P0		2	eilli-	4855.5	924.29	
	VCCRTCPRIM_3P3		, uni		4360.2	924.29	
	VCCPRIM_3P3		CO CO		3864.9	924.29	
	VCCSRAM_1P0		-90 ⁽¹⁾		3369.6	924.29	
	VSS	à	Jan Start St		2874.3	924.29	
	VCCIO	sineu			2379	924.29	
	VSS	uder.		101	1883.7	924.29	
0	VCCSA	6. <u> </u>		inde	1388.4	924.29	
	VSS			ed	8792.21	966.22	
AK30	VCCSA			YG, , ,	893.1	924.29	
	VCC				397.8	924.29	5
	VSS		03/11:2		-97.5	924.29	
AK35	VCCG1		deil.		-592.8	924.29	
AK36	VSS	6	D. T. C.		-1088.1	924.29	
	VCCG1	-siner	<i>P</i>		-1583.4	924.29	
AK40	VSS	nder		24	-2078.7	924.29	
AK41	VCC	0		ino.	-2574	924.29	
	VCCGT	Q -		red	-3069.3	924.29	
AK44	VCCGT			76,11,	-3564.6	924.29	
AK46	VCCGT		10	<u>.</u>	-4059.9	924.29	
AK47	VCCGT		^O 9 _{1i}		-4555.2	924.29	
	VCCGT		delli		-5050.5	924.29	
AK5	VSS		d Will		8299.45	966.22	
AK50	VCCGT	Sine			-5545.8	924.29	
AK51	VCCGT	ndei		2	-6041.1	924.29	
AK54	VSS	ed u.		, une	-6821.17	966.22	
AK56	DDR1_DQ[13] / DDR0_DQ[29]		DDR1_DQ[13]	DDR0_DQ[29]	-7313.93	966.22	
AK58	DDR1_DQ[12] / DDR0_DQ[28]	1	DDR1_DQ[12]	DDR0_DQ[28]	-7806.69	966.22 966.22 966.22 966.22	
AK60	DDR0_DQ[3]		2	<u> </u>	-8299.45	966.22	
AK62	DDR0_DQ[2]		sineu		-8792.21	966.22	
AK64	VDDQ	1	nder.		-9310.37	966.22	
AK7	VSS		d'		7806.69	966.22	
AK9	VSS	nije i			7313.93	966.22	
AL10	GPP_F21 / EMMC_RCLK	nde			7067.55	1288.29	
AL12	GPP_F18 / EMMC_DATA5	ed			6574.79	1288.29	
AL15	VCCDSW_3P3			cin ^{eo}	5846.1	1483.09	
AL16	VSS	1		der	5350.8	1483.09	
AL18	VCCPRIM_1P0		6	Un	4855.5	1483.09	
	186 undefined undefine	ľà-	ned undefined		Datasheet, V	1483.09 1483.09 1483.09 Volume 1 of 2	
	d un-	ude.			Jefin -		
		du			20-		

/CCRTCPRIM_3P3 DCPDSW_1P0 /SS /CCSRAM_1P0		_ unde	ineo	4360.2 9038.59	1483.09 1288.29	
/SS		- unde		9038.59	1288 29	
		<u></u> Ui			1200.25	1170
/CCSRAM_1P0				3864.9	1483.09	nde
		sines		3369.6	1483.09	
/SS		de.		2874.3	1483.09	
/CC10	ed o			2379	1483.09	
/SS	efine			1883.7	1483.09	
/CCSA	inos		den	1388.4	1483.09	
/SS	3		d une	893.1	1483.09	
VCC ASIM			sine	397.8	1483.09	
/SS une		0		-97.5	1483.09	ille,
/CCG1		dui		-592.8	1483.09	noc
/SS		sine		-1088.1	1483.09	¥.
/CCG1		nde		-1583.4	1483.09	
JSB2P_3	, d			8545.83	1288.29	
/SS	efine			-2078.7	1483.09	
/CC	inos		den	-2574	1483.09	
/SS	<u>}0</u>		4 uns	-3069.3	1483.09	
/ss			since	-3564.6	1483.09	
/SS			Ser.	-4059.9	1483.09	.0
/SS		dun		-4555.2	1483.09	Inde
/SS		sine		-5050.5	1483.09	
/SS		nde		-5545.8	1483.09	
/SS	6			-6041.1	1483.09	
/SS	10fine			-6574.79	1288.29]
DDR1_DQ[8] / DDR0_DQ[24]	Inos	DDR1_DQ[8]	DDR0_DQ[24]			
DDR1_DQ[9] / DDR0_DQ[25]	e	DDR1_DQ[9]	DDR0_DQ[25]	-7560.31	1288.29]
/SS	÷		sinet	-8053.07	1288.29]
JSB2N_3		1	der.	8053.07	1288.29	
DDR0_DQ[6]		-d ui		-8545.83	1288.29	undf
DDR0_DQ[7]		sine		-9038.59	1288.29	0
GPP_F22 / EMMC_CLK		nder		7560.31	1288.29	1
DCPDSW_1P0		<u> </u>		9310.37	1610.36	1
GPP_F12 / EMMC_CMD	infine			6821.17	1610.36	1
/CCDSW_3P3	Inoc			6328.41	1615.44	
JSB2N_2	ed -			8792.21	1610.36	1
JSB2P_2			sinec	8299.45	1610.36	1
/SS			gen	-6821.17	1610.36	
DDR1_DQ[7] / DDR0_DQ[23]		DDR1_DQ[7]	DDR0_DQ[23]	-7313.93	1610.36	<u>.</u>
	/SS //CCSA /SS //CC /SS //CCG1 /SS /CCG1 /SS /CCG1 /SS //CCG1 /SS //SS /SS /SS /SS /SS /SS /SS /SS /	/SS ////////////////////////////////////	YSS Image: CCCSA YSS Image: CCC YSS Image: CCCG1 YSS Image: CCCG1	KS Image: Constraint of the second seco	KSS Image: Marking the mar	RSS Image: state sta

ed undefined undefined Y-Processor Ball List (Sheet 9 of 40) Table 9-2.

U/U-Quad Core/YProcessor BallInformation



Datasheet, Volume 1 of 2 - d undefined

1932.43

-8053.07

led undefined

Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]
AM58	DDR1_DQ[6] / DDR0_DQ[22]		DDR1_DQ[6]	DDR0_DQ[22]	-7806.69	1610.36
AM60	DDR0_DQ[8]		Ś	e i	-8299.45	1610.36
AM62	DDR0_DQ[9]		d un		-8792.21	1610.36
AM64	Vss		sinet		-9310.37	1610.36
AM7	GPP_F10 / I2C5_SDA / ISH_I2C2_SDA		der		7806.69	1610.36
AM9	GPP_F17 / EMMC_DATA4	, bo			7313.93	1610.36
AN10	GPP_F15 / EMMC_DATA2	fine			7067.55	1932.43
AN12	GPP_F13 / EMMC_DATA0	nde		20 ¹	6574.79	1932.43
AN15	VCCPGPPG). ().		, unu	5846.1	2041.89
AN16	Vss			tine ⁰	5350.8	2041.89
AN18	vss			Ve.,	4855.5	2041.89
AN19	Vss		d Un		4360.2	2041.89
AN2	VCCPGPPF		sinet		9038.59	1932.43
AN21	VSS		de'		3864.9	2041.89
AN23	VCCSRAM_1P0	6-			3369.6	2041.89
AN24	VSS	fine			2874.3	2041.89
AN26	VCCIO	nde		عد	2379	2041.89
AN27	VSS	0		, uno-	1883.7	2041.89
AN29	VCCSA	v		eneo.	1388.4	2041.89
AN30	VCCSA			dein	893.1	2041.89
AN32	vcc		20		397.8	2041.89
AN33	VSS		sineu		-97.5	2041.89
AN35	VCCG1		dell		-592.8	2041.89
AN36	vss				-1088.1	2041.89
AN38	VCCG1	Sine			-1583.4	2041.89
AN4	GPP_F8 / I2C4_SDA	nde		2	8545.83	1932.43
AN40	VSS	d V.		, unu	-2078.7	2041.89
AN41	vcc	0		ineo.	-2574	2041.89
AN43	VCCGT			-961	-3069.3	2041.89
AN44	VCCGT		21	110 Alexandre	-3564.6	2041.89
AN46	VCCGT		sineu		-4059.9	2041.89
AN47	VCCGT		dell		-4555.2	2041.89
AN49	VCCGT		<i>d v</i> ¹		-5050.5	2041.89
AN50	VCCGT	nija_			-5545.8	2041.89
AN51	VCCGT	nde			-6041.1	2041.89
AN53	DDR0_VREF_DQ	ed u.		, un	-6574.79	1932.43
AN55	DDR1_DQ[3] / DDR0_DQ[19]		DDR1_DQ[3]	DDR0_DQ[19]	-7067.55	1932.43
AN57	DDR1_DQ[2] / DDR0_DQ[18]		DDR1_DQ[2]	DDR0_DQ[18]	-7560.31	1932.43
	Vicc			111	0052.07	1022.42

er and undefined undefin

Y-Processor Ball List (Sheet 10 of 40) Table 9-2.

VSS

AN59



Idefined undefine U/U-Quad Core/YProcessor BallInformation

cinter defined un

Table 9-2.

	undefine		def	ined			stined
	U/U-Quad Core/YProcessor BallInform	ation	defined undef		(ir	ntel	
2	etineo				d une		
onu da	Table 9-2. Y-Processor Ball	100-		Non-Interleaved	N Frank	N From 1	
ne Ball #	Ball Name	LPDDR3	Interleaved (IL)	(NIL)	X [um]	Y [um]	
AN6	GPP_F9 / I2C4_SCL			einer	8053.07	1932.43	60
AN61	DDR0_DQ[12]		de		-8545.83	1932.43	Stine
AN63	DDR0_DQ[13]		du		-9038.59	1932.43	
AN8	GPP_F20 / EMMC_DATA7		sine		7560.31	1932.43	
AP1	VCCPGPPF		00e		9310.37	2254.5	
AP11	GPP_F2 / I2S2_TXD	ed v			6821.17	2254.5	
AP13	VCCPGPPG	lefin			6328.41	2259.58	
AP3	GPP_F4 / I2C2_SDA	inas		der.	8792.21	2254.5	
AP5	GPP_F6 / I2C3_SDA			d une	8299.45	2254.5	
AP54	VSS			sineu	-6821.17	2254.5	
AP56	DDR1_DQSN[0] / DDR0_DQSN[2]		DDR1_DQSN[0]	DDR0_DQSN[2]	-7313.93	2254.5	atine
AP58	DDR1_DQSP[0] / DDR0_DQSP[2]		DDR1_DQSP[0]	DDR0_DQSP[2]	-7806.69	2254.5	
AP60	DDR0_DQSP[1]		sines		-8299.45	2254.5	
AP62	DDR0_DQSN[1]		de		-8792.21	2254.5	
AP64	VSS	6			-9310.37	2254.5	
AP7	GPP_F5 / I2C2_SCL	fine			7806.69	2254.5	
AP9	GPP_F14 / EMMC_DATA1	noc		194	7313.93	2254.5	
AR10	VSS			, uns	7067.55	2576.58	
AR12	VSS			the Co	6574.79	2576.58	
AR15	vss			10th	5846.1	2600.69	nia
AR16	VCCPRIM_CORE		d UN	w	5350.8	2600.69	
AR18	VSS		sineu		4855.5	2600.69	
AR19	VCCRTC		delli		4360.2	2600.69	
AR2	VSS	6			9038.59	2576.58	
AR21	VCCPRIM_1P0	sines			3864.9	2600.69	
AR23	VCCSRAM_1P0	nder.		10	3369.6	2600.69	
AR24	VSSIO_SENSE	0.0.		Inou	2874.3	2600.69	
AR26	VCCIO			ed	2379	2600.69	
AR27	VSS			20111	1883.7	2600.69	Indefin
AR29	VCCSA				1388.4	2600.69	gerr
AR30	VSS	+	ined i		893.1	2600.69	<i>71.</i>
AR30	VCC		det.		397.8	2600.69	
AR32 AR33	VSS	2	UN.		-97.5	2600.69	
AR35	VCCG1	sine			-592.8	2600.69	
AR35 AR36	Vss	olen.			-1088.1	2600.69	
AR38	VCCG1	d un		bn.	-1583.4	2600.69	
AR30	VSS	e		ed v.	8545.83	2576.58	
				i etino		2570.30	
		-		0~		2000.09	, det
AR40 AR41	VSS VCC Datasheet, Volume 1 of 2	ned undefine	d undefined "	NOCKIN,	-2078.7 -2574	2576.58 2600.69 2600.69 189	undf
stined	undefill	ed undefin.		a une	lefiner		



Table 9-2.

	(intel) red undefine		, und			odefi
	(intel)		aneo u/	U-Quad Core/YProc	essor Ball	Information
			dell			etine
	eine	d 1			nu.	
	Table 9-2. Y-Processor Ball	List (Sheet 12	2 of 40)			
Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved	X [um]	Y [um]
	et	LFDDRS	Intelleaved (IL)	(NIL)		
	VSS			sines	-3069.3	2600.69
	VSS			6.	-3564.6	2600.69
	VSS		ed u.		-4059.9	2600.69
	VSS		stine		-4555.2	2600.69
	VSS		uno ^c		-5050.5	2600.69
	VSS	ed			-5545.8	2600.69
	VSS	Jefli.			-6041.1	2600.69
~O·	DDR_VREF_CA	JUNY			-6574.79	
	DDR1_DQ[1] / DDR0_DQ[17]	,	DDR1_DQ[1]	DDR0_DQ[17]	-7067.55	
	DDR1_DQ[4] / DDR0_DQ[20]		DDR1_DQ[4]	DDR0_DQ[20]	-7560.31	2576.58
	VSS			00		2576.58
	VSS		ed v.		8053.07	2576.58
	DDR0_DQ[11] DDR0_DQ[14]	-	Lefill-		-8545.83 -9038.59	
	VSS	-	uno		7560.31	2576.58
	VCCPGPPA	ine ⁽			9310.37	2898.65
	GPP_F0 / I2S2_SCLK	defin			6821.17	2898.65
	GPP_F1 / I2S2_SFRM	June		nde	6328.41	2903.73
	VCCSPI	80		ed u.	5846.1	3159.49
-	VCCPRIM_CORE			16110	5350.8	3159.49
	DCPRTC			10-	4855.5	3159.49
	VCCRTC		- ned		4360.2	3159.49
	VCCPRIM_1P0		defin.		3864.9	3159.49
	VCCHDA		d une		3369.6	3159.49
	VCCIO_SENSE	Prija			2874.3	3159.49
	VCCIO	10001			2379	3159.49
AT27	VSS	d'un		no uno	1883.7	3159.49
AT29	VCCSA_DDR			tined.	1388.4	3159.49
AT3	SPI0_MOSI			detti	8792.21	2898.65
AT30	VCCSA_DDR	1	2	<u>757</u>	893.1	3159.49 3159.49 2898.65 3159.49
AT32	VCC		finel		397.8	3159.49
AT33	VCC		.nde.		-97.5	3159.49
AT35	VCC		0		-592.8	3159.49
AT36	vcc	. Still			-1088.1	3159.49
AT38	VCC	Inor			-1583.4	3159.49
	VCC	hed t		4 UN	-2078.7	3159.49
	VCC			sinec	-2574	3159.49
	VCCGT			der.	-3069.3	3159.49
AT44	VCCGT		6-	U.	-3564.6	3159.49
	190		ned undefined	[Datasheet, '	3159.49 3159.49 3159.49 Volume 1 of 2
	d un	nder			retition	



	Indefine		10 ^f	Ined			lefined U
	U/U-Quad Core/YProcessor BallInform	ation	idefined undef		(ir	ntel)e, .
	Table 9-2. Y-Processor Ball				ed une		
Ball #		LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]	
AT46	VCCGT			d (int)	-4059.9	3159.49	
AT40	VCCGT		10	ALL C	-4555.2	3159.49	
AT47	VCCGT		un ^{Oc}		-5050.5	3159.49	
AT5	GPP_F3 / I2S2_RXD		the d		8299.45	2898.65	
AT50	VCCGT		ACENT.		-5545.8	3159.49	
AT51	VCCGT	20	00.		-6041.1	3159.49	
AT54	VSS	cineu			-6821.17		
AT56	DDR1_DQ[0] / DDR0_DQ[16]	adell.	DDR1_DQ[0]	DDR0_DQ[16]		2898.65	
AT58	DDR1_DQ[5] / DDR0_DQ[21]	-01 ·	DDR1_DQ[5]	DDR0_DQ[10]	-7806.69		
AT 58	DDR0_DQ[10]				-8299.45		<u> </u>
AT60	DDR0_DQ[15]			Still-		2898.65	
AT62	VDDQ		000		-9310.37		dern
AT64	GPP_F7 / I2C3_SCL		ed -		7806.69	2898.65	
AT7 AT9	GPP_F11/ I2C5_SCL / ISH_I2C2_SCL		defin.		7313.93	2898.65	
AU10	SPI0_CLK		uno.		7067.55	3220.72	
	811.	e o			6574.79	3220.72	
AU12	VCCPGPPA	-de ⁱⁿ		i.	9038.59	3220.72	
AU2 AU4	SPI0_CS0#	JUL		nde,	8545.83	3220.72	
		<u> </u>		ed u.	-6574.79		
AU53	VSS			sin		3220.72	
AU55 AU57			m.			3220.72	detin
AU57 AU59			ed v				JUL
			Jeff The			3220.72	
AU6	SPI0_CS1# VSS		an ^o		8053.07	3220.72 3220.72	
AU61	VSS	ed				3220.72	
AU63	SPI0_CS2#	det III.		_			
AU8		JUNE			7560.31	3220.72	
AV1	VCCPGPPB SPI0 IO2	2		d un	9310.37	3542.79	undefin
AV11				stine	6821.17	3542.79	
AV13	SPI0_IO3			00	6328.41	3542.79	Yetin
AV15	VCCSPI		ed u		5881.62	3573.53	Unc
AV16	VSS		Jefin-		5475.22	3573.53	
AV18	DCPRTC		uno-		4831.08	3573.53	
AV20	VSS		0		4186.94	3573.53	
AV22	VCCHDA	defin.	_		3542.79	3573.53	
AV24	VSS	June		6	2898.65	3573.53	
AV26	VCCIO_DDR	.e ⁰		d un.	2254.5	3573.53	
AV28	VCCIO_DDR			<i>since</i>	1610.36	3573.53	
AV3	GPP_B14 / SPKR			nde.	8792.21	3542.79	refil
AV30	VCCIO_DDR Datasheet, Volume 1 of 2	<u> </u>	ed undefined u	1	966.22	3573.53	J undefil
	undefine	undefin			lefined	underine 191	
Sine				4 Un			



Table 9-2.

	(intel) ed undefine		dunde	stines		defil	
	to be the due			U-Quad Core/YProd	noncor Pol	. Inc.	
			Jefine 0,	o-Quad Core/ IProc	Lessor Ban	1110111141011	
		. 5	nor			Jein.	
. In	Table 9-2. Y-Processor Ball I	ist (Sheet 14-	of 40)		ned un		
Ball #	Ball Name	UN LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]	
AV32	VCCIO_DDR			cin ^{eo}	322.07	3573.53	
AV34	VCCIO_DDR		5-	e	-322.07	3573.53	IUe
AV36	VCCIO_DDR		d un		-966.22	3573.53	
AV38	VCCIO_DDR		Sinou		-1610.36	3573.53	
AV40	VCCIO_DDR		del.		-2254.5	3573.53	
AV42	VCCIO_DDR	6-			-2898.65	3573.53	
AV44	VCCIO_DDR	sines			-3542.79	3573.53	
AV46	VCCIO_DDR	.nde:		76	-4186.94	3573.53	
AV48	VCCIO_DDR	<u>5</u>		, uno-	-4831.08	3573.53	
AV5	GPP_B8 / SRCCLKREQ3#			ed	8299.45	3542.79	
AV50	VCCIO_DDR			AC.	-5475.22	3573.53	
AV52	VSS		, ur		-6119.37	3573.53	
AV54	VSS		oon:		-6821.17	3542.79	
AV56	DDR0_MA[8] / DDR0_CAA[3] /DDR0_MA[8]	DDR0_CAA[3]	der.		-7313.93	3542.79	
	DDR0_BA[2] / DDR0_CAA[5]/ DDR0_BG[0]	DDR0_CAA[5]	3.1.5		-7806.69	3542.79	
	DDR0_RAS# /DDR0_CAB[3]/DDR0_MA[16]	DDR0_CAB[3]			-8299.45	3542.79	
AV62	DDR0_MA[0] /DDR0_CAB[9]/DDR0_MA[0]	DDR0_CAB[9]		10	-8792.21	3542.79	
AV64	VDDQ	0		ino.	-9310.37	3542.79	
AV7	GPP_B9 / SRCCLKREQ4#	Q -		ed	7806.69	3542.79	
	GPP_B6 / SRCCLKREQ1#			76111	7313.93	3542.79	
	GPP_B16 / GSPI0_CLK		1	£0.	7067.55	3864.86	
AW12	GPP_B20 / GSPI1_CLK		Oonia		6574.79	3864.86	
	VSS		dein.		5153.15	3819.91	
	VSS		U.C.		4509.01	3819.91	
	VCCPGPPB	sin ^e			9038.59	3864.86	
	VSS	nder.			3864.86	3819.91	
	VSS	d'h		onu ino	3220.72	3819.91	
	VSS			ed	2576.58	3819.91	
	VCCIO_DDR			7611,	1932.43	3819.91	
	VCCIO_DDR		1	<u> </u>	1288.29	3819.91 3819.91 3819.91 3819.91 3819.91	
	VCCIO_DDR		sineo		644.14	3819.91	
	VCCIO_DDR		derin		0	3819.91	
	VCCIO_DDR		A vn		-644.14	3819.91	
	VCCIO_DDR	7772			-1288.29	3819.91	
	VCCIO_DDR	adel.			-1932.43		
	GPP_B21 / GSPI1_MISO	og n.		77.	8545.83	3864.86	
	VCCIO DDR	19-		ed	-2576.58	3819.91	
	VCCIO_DDR			4111-	-3220.72	3819.91	
۵₩/45	V.		•	unu	-3864.86	3819.91	,6
	192 undefined undefine	Alia	led undefined	1	Datasheet, '	3819.91 3819.91 3819.91 Volume 1 of 2	
	dun	ed unde.		11	ndefille		



Table 9-2.

	d unde.		defined undef			de
	U/U-Quad Core/YProcessor BallInform	ation	sined U.		/ír	ntel
	d unc		ger.			
		d u			nune	
~9e	Table 9-2. Y-Processor Ball	List (Sheet 15	i of 40)			
Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]
AW47	/CCIO_DDR			d (MIL)	-4509.01	3819.91
	/CCIO_DDR		10	(In C		3819.91
	/CCIO_DDR		uno.		-5797.3	3819.91
	DDR1_VREF_DQ		the d			3827.53
	DDR0_MA[9]/DDR0_CAA[1]/DDR0_MA[9]	DDR0_CAA[1]	Je ^f		-7067.55	
	DDR0_MA[7]/DDR0_CAA[4]/DDR0_MA[7]	DDR0_CAA[4]	<u>.</u>			3864.86
	DDR0_MA[5]/DDR0_CAA[0]/DDR0_MA[5]	DDR0_CAA[0]			-8053.07	
	GPP_B17 / GSPI0_MISO	JOEN COL		ii)	8053.07	3864.86
0	DDR0_CKE[3]			inde	-8545.83	
	DDR0_CS#[0]			ed v	-9038.59	
	GPP_B22 / GSPI1_MOSI			C'III	7560.31	3864.86
	GPD4 / SLP_S3#		1 UNO		5994.4	3959.86
	/SS		O O O O O O O O O O O O O O O O O O O		5475.22	4066.29
	RSVD_TP		der.		4831.08	4066.29
	RSVD	6	51 NO		4186.94	4066.29
AY22	IP6	sineo			3542.79	4066.29
AY24	/SS	nder		leit	2898.65	4066.29
AY26	/SS			, unos	2254.5	4066.29
	/SS			ed	1610.36	4066.29
AY30 \	/SS			C.	966.22	4066.29
AY32	/SS		1 UN	V*	322.07	4066.29
	/SS		03013		-322.07	4066.29
	/SS		"gen		-966.22	4066.29
AY38	/SS	6			-1610.36	4066.29
AY40	/SS	Aines			-2254.5	4066.29
AY42	/SS	nde.		فكر	-2898.65	4066.29
AY44	/SS	<u>, 0, 1, 1</u>		, uno-	-3542.79	4066.29
AY46	/ss			cin ^{eo}	-4186.94	4066.29
AY48	/ss			9er.,	-4831.08	4066.29 4066.29 4066.29 4066.29
AY50	/ss		AUT		-5475.22	4066.29
AY52	/SS		finel		-6119.37	4066.29
B10 F	PCIE_RCOMPP		.nde.		7085.58	-7269.23
B12 (CL_RST#	~	9000		6441.44	-7269.23
B15 U	JSB3_2_RXN / SSIC_RXN	fine			5797.3	-7269.23
B17 l	JSB3_4_RXN	Inde		24	5153.15	-7269.23
B19 F	PCIE2_RXN / USB3_6_RXN	ed T		1 UNC	4509.01	-7269.23
B21 F	PCIE4_RXN			sinea	3864.86	-7269.23
B23 F	PCIE6_RXN			<i>den</i>	3220.72	-7269.23
B25 F	PCIE8_RXN / SATA1A_RXN		20		2576.58	-7269.23
	Datasheet, Volume 1 of 2	eine	ad undefined t		od	-7269.23 -7269.23 -7269.23 193
	undefine	d under.		inc	letime	



Table 9-2.

	(intel) and undefine		2	stines			ned
	inted u		ed uno	U-Quad Core/YProd	accor Ball	Information	
	(Intel)		define of	o-quad core/ iProc	essor ban		
		24	JUC.			Je ₁ .	
ini	Table 9-2. Y-Processor Ball	List (Sheet 16	i of 40)	ii.	ned un		
Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]	
B27	PCIE10_RXN			sin ^{eo}	1932.43	-7269.23	
B29	CSI2_DP4		6	C.	1288.29	-7269.23	ING
B3	RSVD		d UN		8881.11	-7111.75	
B31	CSI2_CLKP1		einec.		644.14	-7269.23	
B33	CSI2_DP7		de,		0	-7269.23	
B35	CSI2_DP8	6-	<u></u>		-644.14	-7269.23	
B37	CSI2_DP10	AINE			-1288.29	-7269.23	
B39	CSI2_CLKP3			76	-1932.43	-7269.23	
B4	RSVD	d.		uno-	8451.85	-7111.75	
B41	DDI2_TXN[2]	/		ed	-2576.58	-7269.23	
	DDI2_TXN[3]			YG,	-3220.72	-7269.23	
	DDI1_TXN[2]		L UP	0.	-3864.86	-7269.23	
	DDI1_TXN[3]		09/10		-4509.01	-7269.23	
	JTAGX		- Yerlin		-5153.15		
_	PCH_JTAG_TDO	2	UN ^S		-5797.3	-7269.23	
	PCH_JTAG_TCK	inel .			-6441.44		
	PROC_PREQ#	dell			-7085.58	-7269.23	
	VIDALERT#	- dull'		nd ^e	-7777.48		
	eDP_BKLCTL	er~		ed V	8022.59	-7111.75	
	VCCST_PWRGD			1112	-8479.79	-7111.75	
	SKTOCC#			0~	-8881.11		e,
	VCC		- ned		-9310.37		
	GPP_E12 / USB2_OC3#		Yeth.		7593.33	-7111.75	
	VSS		J UNC		9310.37	4186.94	
	VSS	e	0		6821.17	4186.94	
	GPP_B0 / CORE_VID0	defin			6328.41	4186.94	
0	GPD8 / SUSCLK	June		6,,	5797.3		
	RSVD_TP	eu		d V.	5153.15	4312.67	
				Aino		4312.07	
	RSVD			no-	4509.01	4312.67 4312.67 4312.67 4312.67	
	RSVD		ed l	P*	3864.86	4212.67	
	TP5		define-		3220.72	4312.67	
	VDDQ		uno-		2576.58	4312.67	
	VDDQ		e ^{0. –}		1932.43	4312.67	
	VDDQ	Aefill			1288.29	4312.67	
	VSS	unu			8792.21	4186.94	
	VDDQ	ne ⁰		d ul	644.14	4312.67	
	VDDQ			sines	0	4312.67	
	VDDQ			de.	-644.14	4312.67	20
BA37	VDDQ		6	O.	-1288.29	4312.67	
	194 194 194	10	ned undefined	I	Datasheet, '	4312.67 4312.67 4312.67 Volume 1 of 2	
	du.	nde			YetIII.		
		du		· · · · · · · · · · · · · · · · · · ·	74.		



Table 9-2.

	undefilt		def	Iner			fine
	U/U-Quad Core/YProcessor BallInforma	ation	Idefined undef		(ir	ntel	ý*
	atined	ed L			d und		
ind and	Table 9-2. Y-Processor Ball L	ist (Sheet 17	7 of 40)	A Stin	30.	1 1	
Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]	
BA39	VDDQC			aneo	-1932.43	4312.67	
BA41	VDDQ		de		-2576.58	4312.67	SILL
BA43	VDDQ		d un		-3220.72	4312.67	
BA45	VDDQ		fine		-3864.86	4312.67	
BA47	VDDQ		ndie		-4509.01	4312.67	
BA49	VDDQ	ed v			-5153.15	4312.67	
BA5	VSS	efine			8299.45	4186.94	
BA51	VDDQ	Inor		den	-5797.3	4312.67	
BA53	vss			Jun	-6441.44	4320.29	
BA56	DDR0_MA[12]/DDR0_CAA[6]/DDR0_MA[12]	DDR0_CAA[6]		sinet	-7313.93	4186.94	
BA58	vss		6	C I		4186.94	, efir
BA60	DDR0_CKN[1]		d un		-8299.45		
BA62	DDR0_CKP[1]		sino			4186.94	
BA64	VSS		nde			4186.94	
BA7	VSS	ed			7806.69	4186.94	
BA9	VSS	1efille		<i></i>	7313.93	4186.94	
BB10	GPP_B5 / SRCCLKREQ0#	unos		del	7067.55	4509.01	
BB12	GPP_B1 / CORE_VID1			d un	6548.63	4559.05	
BB14	RSVD			sinec	6119.37	4559.05	
BB16	GPD7 / RSVD			le.	5475.22	4559.05	
BB18	RSVD		du.		4831.08	4559.05	10.5
BB2	GPP_B19 / GSPI1_CS#		Stine		9038.59	4509.01	
BB20	VSS		inde		4186.94	4559.05	
BB22	VSS	ed			3542.79	4559.05	
BB24	VSS	Jefill		-	2898.65	4559.05	
BB26	VSS	un ^o			2254.5	4559.05	
BB28	VSS	0		d UII.	1610.36	4559.05	
BB30	VSS			- since	966.22	4559.05	
BB32	VSS			de	322.07	4559.05	ndef
BB34	VSS		ed V		-322.07	4559.05	
BB36	VSS		A GITT		-966.22	4559.05	
BB38	VSS GPP_B18 / GSPI0_MOSI		un ^{o-}		-1610.36	20.	
BB4	VSS		0		8545.83	4509.01 4559.05	
BB40	VSS	defini			-2254.5	4559.05	
BB42	VSS	Jun		6			
BB44	VSS	200		d U'	-3342.79	4550.05	
BB46 BB48	VSS			Jetine .	-4100.94	4550.05	
BB48 BB50	1 V.			noe	-4031.00	4559.05	6
	Datasheet, Volume 1 of 2	00	ed undefined t		6	4559.05 4559.05 4559.05 4559.05 195	Uli
	undefine	od undern		ind	efines		



Table 9-2.

	ened undefine		24	stineo			
	red un		ed uno.			unden	
	(intel)		etine u/	U-Quad Core/YProc	cessor Ball	Information	
			nde			lef11.	
	atine				y nu		
n.	Table 9-2. Y-Processor Ball I	List (Sheet 18	of 40)		nec.		
Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]	
BB52	VSS			ed	-6119.37	4559.05	
BB54	VSS			C.	-6763.51	4559.05	10
BB57	DDR0_CKE[0]		4 UN		-7560.31	4509.01	
BB59	VSS		cineu		-8053.07	4509.01	
BB6	GPP_B23 / SML1ALERT# / PCHHOT#		delli		8053.07	4509.01	
BB61	DDR0_MA[2] /DDR0_CAB[5]/DDR0_MA[2]	DDR0_CAB[5]			-8545.83	4509.01	
BB63	DDR0_MA[3]	sines			-9038.59	4509.01	
BB8	GPP_B13 / PLTRST#	nder		10	7560.31	4509.01	
20	EMMC_RCOMP	d JI.		, unos	9310.37	4831.08	
	 GPP_B4 / CPU_GP3			ed -	6695.44	4978.4	
	GPD11 / LANPHYPC			YG,	5797.3	4805.43	
BC17	VSS		1 UP	0.	5153.15	4805.43	
BC19	RSVD		O S ni		4509.01	4805.43	
BC21	DDR1_DQ[62]		dein.		3864.86	4805.43	
	DDR1_DQ[59]	à	0.(1~		3220.72	4805.43	
BC25	DDR1_DQ[55]	sines			2576.58	4805.43	
	DDR1_DQ[51]	nde''		10	1932.43	4805.43	
0	VSS	0		ino.	1288.29	4805.43	
BC3	GPP_B15 / GSPI0_CS#			ed t	8792.21	4831.08	
	DDR1_MA[1] /DDR1_CAB[8]/DDR1_MA[1]	DDR1_CAB[8]		Ye, I.	644.14	4805.43	
	DDR1_BA[0] /DDR1_CAB[4]/DDR1_BA[0]	DDR1_CAB[4]	ن س	0.	0	4805.43	6
BC35	DDR1_ODT[0]		^O Snia		-644.14	4805.43	
	DDR1_WE#/DDR1_CAB[2]/DDR1_MA[14]	DDR1_CAB[2]	deili		-1288.29	4805.43	
BC39	DDR0_DQ[33] / DDR1_DQ[1]		DDR0_DQ[33]	DDR1_DQ[1]	-1932.43	4805.43	
BC41	DDR0_DQ[32] / DDR1_DQ[0]	-fine'	DDR0_DQ[32]	DDR1_DQ[0]	-2576.58	4805.43	
BC43	DDR0_DQ[40] / DDR1_DQ[8]	nder.	DDR0_DQ[40]	DDR1_DQ[8]	-3220.72	4805.43	
BC45	DDR0_DQ[44] / DDR1_DQ[12]	du	DDR0_DQ[44]	DDR1_DQ[12]	-3864.86	4805.43	
	VSS			ed -	-4509.01	4805.43	
	DDR0_DQ[26] / DDR0_DQ[42]		DDR0_DQ[26]	DDR0_DQ[42]	-5153.15	4805.43 4805.43 4805.43 4831.08	
	GPP_B10 / SRCCLKREQ5#		2/		8299.45	4831.08	
	DDR0_DQ[24] / DDR0_DQ[40]		DDR0_DQ[24]	DDR0_DQ[40]	-5797.3	4805.43	
	DDR0_DQ[20] / DDR0_DQ[36]		DDR0_DQ[20]	DDR0_DQ[36]	-6441.44		
	DDR0_DQ[17] / DDR0_DQ[33]		DDR0_DQ[17]	DDR0_DQ[33]	-7085.58	4805.43	
	DDR0_CKE[1]	eine			-7806.69	4831.08	
	DDR0_CKP[0]	nde''				4831.08	
	DDR0_CKN[0]	dui		nı.	-8792.21	4831.08	
	DDR_RCOMP[2]			ed	-9310.37	4831.08	
	GPP_B11 / EXT_PWR_GATE#			. <u>16</u> 11.	7806.69	4831.08	
BC9	GPP_B12 / SLP_S0#		2	UNC	7313.93	4831.08	,6
	196	ined undefin	ed undefined		Datasheet, "	4831.08 4831.08 4831.08 Volume 1 of 2	
	d u.	Inoc			9eun		
				ى .			



Table 9-2.

	undefine		de	ined			ofined U
	U/U-Quad Core/YProcessor BallInform	ation	defined undef		(ir	ntel	9e.
	stined				dune		
und	Table 9-2. Y-Processor Ball I	ist (Sheet 19	of 40)	Sin	S		
Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]	
BD10	GPP_B7 / SRCCLKREQ2#			nea	7067.55	5148.58	-6'
BD14	GPD1 / ACPRESENT		-96		6119.37	5051.81	since
BD16	GPD0 / BATLOW#		d un		5475.22	5051.81	ge.
BD18	RSVD		sinou		4831.08	5051.81	
BD2	GPP_A19 / ISH_GP1		ger.		9038.59	5153.15	
BD20	VSS	d'u			4186.94	5051.81	
BD22	DDR1_DQSP[7]	sines			3542.79	5051.81	
BD24	DDR1_DQ[57]	ndei		16/11	2898.65	5051.81	
BD26	DDR1_DQSN[6]	0.		, unos	2254.5	5051.81	
BD28	DDR1_DQ[49]			ed	1610.36	5051.81	A
BD30	DDR1_PAR		2	6	966.22	5051.81	
BD32	DDR1_CKN[1]		1 Uno		322.07	5051.81	dei
BD34	DDR1_ALERT#		ine ⁰		-322.07	5051.81	
BD36	 DDR1_BA[1] /DDR1_CAB[6]/DDR1_BA[1]	DDR1_CAB[6]	- detin		-966.22	5051.81	
BD38	VSS				-1610.36	10.	
BD4	GPP_A23 / ISH_GP5	sineu			8545.83	5153.15	
BD40	DDR0_DQSN[4] / DDR1_DQSN[0]	delli	DDR0_DQSN[4]	DDR1_DQSN[0]	-2254.5	5051.81	
BD42	DDR0_DQ[37] / DDR1_DQ[5]	UN.	DDR0_DQ[37]	DDR1_DQ[5]	-2898.65		
BD42	DDR0_DQSN[5] / DDR1_DQSN[1]		DDR0_DQSN[5]	DDR1_DQSN[1]	-3542.79		
BD44 BD46	DDR0_DQ[41] / DDR1_DQ[9]		DDR0_DQ[41]	DDR1_DQ[9]	-4186.94		ine
BD40 BD48	DDR0_DQ[31] / DDR0_DQ[47]		DDR0_DQ[31]	DDR0_DQ[47]		5051.81	dein.
	DDR0_DQ[31] / DDR0_DQ[47]		DDR0_DQSP[3]	DDR0_DQSP[5]		5051.81	une
	DDR0_DQ3r[3] / DDR0_DQ3r[3]		DDR0_DQ[22]	DDR0_DQ[38]		5051.81	
BD52	DDR0_DQ[22] / DDR0_DQ[36]		DDR0_DQ[22]	DDR0_DQ[38]		5051.81	
BD54	VSS	ine ⁰			-7407.66	*	
BD56					100		
BD59	DDR0_MA[11] /DDR0_CAA[7] / DDR0_MA[11]	DDR0_CAA[7]		nde	-8133.08	5237.48	
BD6	GPP_B2 / VRALERT#			du	8053.07	5153.15	
BD61	DDR0_MA[15] /DDR0_CAA[8]/DDR0_ACT#	DDR0_CAA[8]		efine	-8545.83	5153.15	undefine
BD63	VSS			0	-9038.59	5153.15	Yethin
BD8	GPP_B3 / CPU_GP2		ed u		7560.31	5153.15	un
BE12	vss		10ftm		6441.44	5298.19	
BE15	GPD2 / LAN_WAKE#		uno		5797.3	5298.19	
BE17	GPD6 / SLP_A#	- el			5153.15	5298.19	
BE19	RSVD	ACTIVICE ACTIVICE		1	4509.01	5298.19	
BE21	DDR1_DQ[63]	, unu			3864.86	5298.19	
BE23	DDR1_DQ[60]	60		-2011	3220.72	5298.19	
BE25	DDR1_DQ[54]			fines	2576.58	5298.19	
BE27				nder	1932.43	5298.19 5298.19 5298.19 5298.19	defin
	efinor		d undefined "		1		dunc
	unde		defin			efine	
	Datasheet, Volume 1 of 2		dur.			197	
	undefine				60		
	un	nder.			stine		
		1 UN.		n.			

/	nte	
(1		
	20	

	(intel) red undefine		ed unde			indefi
	(intel)			U-Quad Core/YProc	cessor Ball	Information
			der.			efine
	einee	ed u			, un	
	Table 9-2. Y-Processor Ball I	ist (Sheet 20	of 40)			
Ball #	Ball Name	UNOU LPDDR3	Interleaved (IL)	Non-Interleaved	X [um]	Y [um]
	e ⁰	EFBORS	Interleaved (IL)	(NIL)		
	VSS			sines	1288.29	5298.19
-	VSS		ind.		644.14	5298.19
	VSS		ed V.		0	5298.19
	VSS		Stine		-644.14	5298.19
	DDR1_CAS#/DDR1_CAB[1]/DDR1_MA[15]	DDR1_CAB[1]	noc		-1288.29	5298.19
	DDR0_DQ[35] / DDR1_DQ[3]	ed	DDR0_DQ[35]	DDR1_DQ[3]	-1932.43	
	DDR0_DQ[39] / DDR1_DQ[7]	Jefin.	DDR0_DQ[39]	DDR1_DQ[7]		5298.19
0	DDR0_DQ[45] / DDR1_DQ[13]	un	DDR0_DQ[45]	DDR1_DQ[13]	-3220.72	
	DDR0_DQ[46] / DDR1_DQ[14]	V	DDR0_DQ[46]	DDR1_DQ[14]		
	VSS			din series	-4509.01	5298.19
	DDR0_DQ[27] / DDR0_DQ[43]		DDR0_DQ[27]	DDR0_DQ[43]	-5153.15	20
	DDR0_DQ[25] / DDR0_DQ[41]		DDR0_DQ[25]	DDR0_DQ[41]	-5797.3	5298.19
	DDR0_DQ[19] / DDR0_DQ[35]		DDR0_DQ[19]	DDR0_DQ[35]	-6441.44	
	DDR0_DQ[16] / DDR0_DQ[32]		DDR0_DQ[16]	DDR0_DQ[32]		5298.19
	DDR0_CKE[2]	ed			-7729.73	
	SD_RCOMP	defini			9310.37	5475.22
0	GPP_A18 / ISH_GP0	June			6763.51	5544.57
	GPD3 / PWRBTN#	3.01		d Un	6119.37	5544.57
	GPD5 / SLP_S4#			in ^o	5475.22	5544.57
-	RSVD			de	4831.08	5544.57
BF20			ed v		4186.94 3542.79	5544.57
	DDR1_DQSN[7]		Actility			5544.57 5544.57
	DDR1_DQ[56]		unos		2898.65 2254.5	5544.57
	DDR1_DQSP[6]	e				5544.57
	DDR1_DQ[48] GPP_A7 / PIRQA#	detin			1610.36 8792.21	5475.22
	DDR1_MA[2] /DDR1_CAB[5]/DDR1_MA[2]	DDR1_CAB[5]		6,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	966.22	554453
	DDR1_MA[2]/DDR1_CAB[3]/DDR1_MA[2]	PRIT CUD[2]		du.	322.07	5544.57 5544.57 5544.57 5544.57
	DDR1_RAS# /DDR1_CAB[3]/DDR1_MA[16]	DDR1_CAB[3]		1610-	-322.07	5544.57
	DDR1_MA[0] /DDR1_CAB[9]/DDR1_MA[0]	DDR1_CAB[9]		n0-	-966.22	5544.57
	VSS		ed		-1610.36	5544.57
	DDR0_DQSP[4] / DDR1_DQSP[0]		DDR0_DQSP[4]	DDR1_DQSP[0]	-2254.5	5544.57
	DDR0_DQ[36] / DDR1_DQ[4]		DDR0_DQ[36]	DDR1_DQ[4]	-2898.65	5544.57
	DDR0_DQSP[5] / DDR1_DQSP[1]	9012	DDR0_DQSP[5]	DDR1_DQSP[1]		5544.57
	DDR0_DQ[47] / DDR1_DQ[15]	adell.	DDR0_DQ[47]	DDR1_DQ[15]		5544.57
-	DDR0_DQ[30] / DDR0_DQ[46]	d'u''	DDR0_DQ[30]	DDR0_DQ[46]	0	5544.57
					8299.45	
	DDR0_DQSN[3] / DDR0_DQSN[5]		DDR0_DQSN[3]	DDR0_DQSN[5]		5475.22 5544.57 5544.57
BF52			DDR0_DQ[23]	DDR0_DQ[39]	-6119.37	5544.57
				((*)	1	
	Inde		defin			sinet
	198	ined undefin	dun	1	Datasheet, V	Volume 1 of 2
	defin.	275				9.0.
	une	der			sine	



Table 9-2.

	a undefine		ndef	Inec			ine
	U/U-Quad Core/YProcessor BallInform	ation	defined undef		(ir	ntel	
6	Table 9-2. Y-Processor Ball I	ed th			ed une		
Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]	
BF54	DDR0_DQSP[2] / DDR0_DQSP[4]		DDR0_DQSP[2]	DDR0_DQSP[4]	-6763.51	5544.57	
BF56	VSS				-7407.66		
BF59	VSS		, uno-		-8163.56	1	
BF62	DDR0_MA[6] /DDR0_CAA[2] /DDR0_MA[6]	DDR0_CAA[2]	ine ⁰			5475.22	
BF64	DDR_RCOMP[0]		- Defin		-9310.37		
BF7	GPP_A11 /PME#	10 1	<u>.</u>		7806.69	5475.22	
BF9	GPP_A15 / SUSACK#	sineu			7308.85	5480.3	
BG10	GPP_A3 / LAD2 / ESPI_IO2	-dell'		in a start	7170.42	5890.26	
BG12	VSS	<i>7</i> 1.		inde	6441.44	5790.95	
BG15	VSS			ed	5797.3	5790.95	
BG17	VSS			C	5153.15	5790.95	
BG19	INTRUDER#		, uno		4509.01	5790.95	e,
BG2	VSS		ine ^O		9038.59	5797.3	
BG21	DDR1_DQ[58]		det li		3864.86	5790.95	
BG23	DDR1_DQ[61]		310		3220.72	5790.95	
	DDR1_DQ[50]	sineu			2576.58	5790.95	
BG27	DDR1_DQ[52]	ole'l'		i la c	1932.43	5790.95	
BG29	VSS	N'		inde	1288.29	5790.95	
BG31	DDR1_MA[7] /DDR1_CAA[4] /DDR1_MA[7]	DDR1_CAA[4]		ed	644.14	5790.95	
	DDR1_CKE[2]			Sill'	0	5790.95	
	DDR1_MA[10] /DDR1_CAB[7]/	DDR1_CAB[7]	, un	0	-644.14	5790.95	
BG35	DDR1_MA[10] DDR1_MA[13] /DDR1_CAB[0] /	DDR1_CAB[0]	sined		-1288.29	dui	
BG37	DDR1_MA[13]		nde.			1efil!	
BG39	DDR0_DQ[38] / DDR1_DQ[6]	6	DDR0_DQ[38]	DDR1_DQ[6]	-1932.43	5790.95	
BG4	VSS	Ains			8545.83	5797.3	
BG41	DDR0_DQ[34] / DDR1_DQ[2]	mais	DDR0_DQ[34]	DDR1_DQ[2]	-2576.58	5790.95	
BG43	DDR0_DQ[42] / DDR1_DQ[10]	0	DDR0_DQ[42]	DDR1_DQ[10]		5790.95	
BG45	DDR0_DQ[43] / DDR1_DQ[11]		DDR0_DQ[43]	DDR1_DQ[11]		5790.95	nde
BG47	RSVD_TP			9e1.		5790.95	
BG49	DDR0_DQ[29] / DDR0_DQ[45]		DDR0_DQ[29]	DDR0_DQ[45]		5790.95	
BG51	DDR0_DQ[28] / DDR0_DQ[44]		DDR0_DQ[28]	DDR0_DQ[44]	-5797.3	5790.95	
BG53	DDR0_DQ[18] / DDR0_DQ[34]		DDR0_DQ[18]	DDR0_DQ[34]	-6441.44	101	
BG55	DDR0_DQ[21] / DDR0_DQ[37]		DDR0_DQ[21]	DDR0_DQ[37]		5790.95	
BG57	DDR0_ALERT#	-stine				5790.95	
BG6	VSS	inos		-	8053.07	5797.3	
BG61	DDR0_MA[14] /DDR0_CAA[9]/ DDR0_BG[1]	DDR0_CAA[9]		4 Une	-8545.83	5797.3	
BG63	VSS			sineu	-9038.59	5797.3	
BG8	vss			den	7560.31	5797.3	
BH11	GPP_A8 / CLKRUN#		-010		6763.51	6037.33	nd
	Datasheet, Volume 1 of 2	ating	ed undefined u		ned	5797.3 5797.3 6037.33 199	
	undefine	ed unde.		und	lefin.		

Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]	
BH14	GPD10 / SLP_S5#			4in ^{eo}	6119.37	6037.33	d U
BH16	GPD9 / SLP_WLAN#		Ś	et i	5475.22	6037.33	since
BH18	SRTCRST#		d un		4831.08	6037.33	nde
BH20	VSS		sinet		4186.94	6037.33	0.1
BH22	VSS		de'		3542.79	6037.33	
BH24	VSS	6	0		2898.65	6037.33	
BH26	VSS	fine			2254.5	6037.33	
BH28	VSS	nde		26	1610.36	6037.33	
BH30	DDR1_CKE[3]) U.		, uno	966.22	6037.33	
BH32	VSS			. neo	322.07	6037.33	
BH34	VSS			Veri.	-322.07	6037.33	sinet
BH36	VSS		100	0.	-966.22	6037.33	nder
BH38	VSS		O90ii		-1610.36	6037.33	U
BH40	VSS		-dein.		-2254.5	6037.33	-
_	VSS	A	DI I		-2898.65	76.	1
	VSS	sine ⁰				6037.33	1
	VSS	delli		10	-4186.94		
	VSS	d'ull'		ind ^e		6037.33	-
	VSS			ed v		6037.33	
	VSS			1112	-6119.37	6037.33	cin ^{e0}
-	VSS			0-		6037.33	-gem.
-	VSS		ed .		-7407.66	6037.33	JUNC
	VSS		Aefil.		-8051.8	6037.33	
	GPP_A20 / ISH_GP2		un ^{o.}		9310.37	6177.03	-
	GPP_A9 / CLKOUT_LPC0 / ESPI_CLK	ine ine	0		7085.58	6283.71	-
	RSMRST#	defi'			6441.44	6283.71	
0	TP1	June		67,	5797.3	6283.71 6283.71	-
	TP2	eu		d'u'	5153.15	6283.71 6283.71	
-	XC.			in the second seco			- ner
	HDA_SYNC / I2S0_SFRM				4509.01	6283.71	- Yelli.
	DDR1_DQ[46] / DDR1_DQ[30]		DDR1_DQ[46]	DDR1_DQ[30]	3864.86	6283.71	d undefine
	DDR1_DQ[43] / DDR1_DQ[27]		DDR1_DQ[43]	DDR1_DQ[27]	3220.72	6283.71	20
	DDR1_DQ[38] / DDR1_DQ[22]		DDR1_DQ[38]	DDR1_DQ[22]	2576.58	6283.71	
	DDR1_DQ[39] / DDR1_DQ[23]		DDR1_DQ[39]	DDR1_DQ[23]	1932.43	6283.71	4
	VSS	Aefil'			1288.29	6283.71	
	GPP_A22 / ISH_GP4	unu		~	8881.11	6253.23	
	DDR1_MA[3]	eo.		d ul	644.14	6283.71	
	DDR1_CS#[1]	P		sines	0	6283.71	_0
0,00	DDR1_MA[11] /DDR1_CAA[7] / DDR1_MA[11]	DDR1_CAA[7]		inde.	-644.14	6283.71	retin
	200	13.	led undefined		Datasheet, V	Volume 1 of .	ned undefine
	dum	uqe.			definit		
		du			10		

Y-Processor Ball List (Sheet 22 of 40) Table 9-2.

d und

(intel) red underme

defined undefined U/U-Quad Core/YProcessor BallInformation

cintel defined un

Table 9-2.

	ned un		defined undef		_	dei
	U/U-Quad Core/YProcessor BallInform	ation			/іг	itel
	d une				.0	
	AINEC	ed u.			4 UMC	
nde	Table 9-2. Y-Processor Ball I	ist (Sheet 23.	of 40)			
Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]
	DDR1_MA[12] /DDR1_CAA[6] / DDR1_MA[12]	DDR1_CAA[6]		ined	-1288.29	6283.71
	DDR0_DQ[63] / DDR1_DQ[47]		DDR0_DQ[63]	DDR1_DQ[47]	-1932.43	6283.71
BJ4	Sx_EXIT_HOLDOFF# / GPP_A12 / BM_BUSY#/ISH_GP6		ed u		8451.85	6253.23
	DDR0_DQ[58] / DDR1_DQ[42]		DDR0_DQ[58]	DDR1_DQ[42]	-2576.58	6283.71
	DDR0_DQ[55] / DDR1_DQ[39]	_ U ^r	DDR0 DQ[55]	DDR1_DQ[39]	A	6283.71
	DDR0_DQ[54] / DDR1_DQ[38]	O9nia	DDR0_DQ[54]	DDR1_DQ[38]	-3864.86	
BJ47	VSS	de ^f	5510-56[51]	0[20]	-4509.01	
	DDR1_DQ[27] / DDR0_DQ[59]	200	DDR1_DQ[27]	DDR0_DQ[59]	-5153.15	
	DDR1_DQ[25] / DDR0_DQ[57]		DDR1_DQ[25]	DDR0_DQ[57]	-5797.3	6283.71
	DDR1_DQ[18] / DDR0_DQ[50]		DDR1_DQ[18]	DDR0_DQ[50]	-6441.44	
	DDR1_DQ[16] / DDR0_DQ[48]		DDR1_DQ[16]	DDR0_DQ[48]		6283.71
	DDR0_CS#[1]		22111_20[10]	551.0_DQ[-10]		6283.71
	GPP_A14 / SUS_STAT#/ ESPI_RESET#		26411-		8022.59	6253.23
	DDR0_WE#/DDR0_CAB[2]/DDR0_MA[14]	DDR0_CAB[2]				6253.23
BJ61	VSS					6253.23
	DDR_RCOMP[1]	dell'				6177.03
0	GPP A2 / LAD1 / ESPI IO1	un		uqe,	7593.33	6253.23
	GPP_A1 / LAD0 / ESPI_IO0	r 		-6 <u>0</u>	6763.51	6530.09
	I2S1_TXD			eine	6119.37	6530.09
	HDA_SDO / I2S0_TXD		11.	<u> </u>	5475.22	6530.09
			ed v.			
	HDA_BLK / I2S0_SCLK VSS		16410-		4831.08 4186.94	6530.09 6530.09
	DDR1_DQSP[5] / DDR1_DQSP[3]		DDR1_DQSP[5]	DDR1_DQSP[3]	4186.94 3542.79	6530.09
		bon.				
	DDR1_DQ[41] / DDR1_DQ[25] DDR1_DQSN[4] / DDR1_DQSN[2]	defin.	DDR1_DQ[41] DDR1_DQSN[4]	DDR1_DQ[25]	2898.65 2254.5	6530.09 6530.09
-0-	DDR1_DQSN[4] / DDR1_DQSN[2] DDR1_DQ[34] / DDR1_DQ[18]	un	DDR1_DQSN[4]	DDR1_DQSN[2] DDR1_DQ[18]	1610.36	6530.09
	DDR1_DQ[34] / DDR1_DQ[18] DDR1_MA[5] /DDR1_CAA[0] /DDR1_MA[5]			DOKT_DO[10]	966.22	6530.09
	764	DDR1_CAA[0]	-	4in ⁶⁻	322.07	6530.09
	DDR1_CKE[1]			00	-322.07	6530.09
	DDR1_MA[4]		ed u.		-966.22	6530.09
	VSS		odefines		-966.22	2
	DDR0_DQSP[7] / DDR1_DQSP[5]		DDR0_DQSP[7]	DDR1_DQSP[5]	-1610.36	6530.09
	DDR0_DQSP[7] / DDR1_DQSP[5] DDR0_DQ[60] / DDR1_DQ[44]		DDR0_DQSP[7]	DDR1_DQ5P[5]	-2254.5	· ·
	DDR0_DQ[80] / DDR1_DQ[44] DDR0_DQSN[6] / DDR1_DQSN[4]	defin.	DDR0_DQ[60]	DDR1_DQ[44]	-2898.65	
-	DDR0_DQ5N[6] / DDR1_DQ5N[4] DDR0_DQ[51] / DDR1_DQ[35]	2 mm	DDR0_DQSN[6]		-4186.94	6530.09
		0			-4831.00	6530.09
	DDR1_DQ[30] / DDR0_DQ[62]		DDR1_DQ[30]	DDR0_DQ[62]	-4031.08	6530.09 6530.09 6530.09 6530.09 201
	DDR1_DQSN[3] / DDR0_DQSN[7]		DDR1_DQSN[3]	DDR0_DQSN[7]	-54/5.22	6520.09
BK52	DDR1_DQ[23] / DDR0_DQ[55]	ed undefine	DDR1_DQ[23]	DDR0_DQ[55]	-9119.37	030.09



Table 9-2.

	undefine		d undefined						
	(intel) red undefine			U-Quad Core/YProd	cessor Ball	Information			
	and un	d U	nde		ini	Jefin			
	Table 9-2. Y-Processor Ball I	ist (Sheet 24	of 40)						
Ball #		LPDDR3	Interleaved (IL)	Non-Interleaved	X [um]	Y [um]			
<u>.</u>				(NIL)					
BK54	DDR1_DQSP[2] / DDR0_DQSP[6]		DDR1_DQSP[2]	DDR0_DQSP[6]	-6763.51	6530.09			
BK56	VSS		n, n		-7407.66	101			
BK59	DDR0_MA[13] /DDR0_CAB[0] / DDR0_MA[13]	DDR0_CAB[0]	ed th		-8102.6	6453.89			
BL1	VSS		4em		9310.37	6631.69			
BL10	GPP_A0 / RCIN#	1	NUC.		7085.58	6776.47			
BL12	I2S1_SFRM	sineu			6441.44	6776.47			
BL15	HDA_SDI0/ I2S0_RXD	der			5797.3	6776.47			
BL17		y Un		inde	5153.15	6776.47			
BL19	HDA_RST# /I2S1_SCLK			ed	4509.01	6776.47			
BL21	DDR1_DQ[47] / DDR1_DQ[31]		DDR1_DQ[47]	DDR1_DQ[31]	3864.86	6776.47			
BL23	DDR1_DQ[44] / DDR1_DQ[28]		DDR1_DQ[44]	DDR1_DQ[28]	3220.72	6776.47			
BL25	DDR1_DQ[35] / DDR1_DQ[19]		DDR1_DQ[35]	DDR1_DQ[19]	2576.58	6776.47			
BL27	DDR1_DQ[37] / DDR1_DQ[21]		DDR1_DQ[37]	DDR1_DQ[21]	1932.43	6776.47			
BL29	VSS	de la			1288.29	6776.47			
BL3	GPP_A21 / ISH_GP3	tines.			8881.11	6682.49			
BL31	VSS	nde.		20	644.14 0	6776.47 6776.47			
BL33	VSS	90.		1 400	-644.14	6776.47			
BL35 BL37	DDR1_MA[8] / DDR1_CAA[3] /DDR1_MA[8]	DDR1_CAA[3]		^O 9713	-1288.29	6776.47			
BL37 BL39	DDR0_DQ[62] / DDR1_DQ[46]		DDR0_DQ[62]	DDR1_DQ[46]		6776.47	Sin		
	GPP_A17 / SD_PWR_EN# / ISH_GP7		DD100_DQ[02]		8451.85	6682.49			
BL41	DDR0_DQ[61] / DDR1_DQ[45]		DDR0_DQ[61]	DDR1_DQ[45]	-2576.58				
BL43	DDR0_DQ[50] / DDR1_DQ[34]		DDR0_DQ[50]	DDR1_DQ[34]		6776.47			
BL45	DDR0_DQ[53] / DDR1_DQ[37]	0	DDR0_DQ[53]	DDR1_DQ[37]		6776.47			
BL47	VSS	10 setting			0	6776.47			
BL49	DDR1_DQ[26] / DDR0_DQ[58]	, unos	DDR1_DQ[26]	DDR0_DQ[58]		6776.47			
BL51	DDR1_DQ[24] / DDR0_DQ[56]	eo -	DDR1_DQ[24]	DDR0_DQ[56]	-5797.3	6776.47			
BL53	DDR1_DQ[19] / DDR0_DQ[51]		DDR1_DQ[19]	DDR0_DQ[51]	-6441.44	6776.47			
BL55	DDR1_DQ[17] / DDR0_DQ[49]		DDR1_DQ[17]	DDR0_DQ[49]	-7085.58	6776.47	defin		
BL57	DDR0_MA[4]		0.	N. T.	-7729.73	6768.85			
BL6	GPP_A13 / SUSWARN# / SUSPWRDNACK		16tine		8022.59	6682.49			
BL61	DDR0_BA[1] /DDR0_CAB[6]/DDR0_BA[1]	DDR0_CAB[6]	, una-		-8451.85	6682.49			
BL62	DDR0_CAS#/DDR0_CAB[1]/DDR0_MA[15]	DDR0_CAB[1]	p		-8881.11	6682.49			
BL64	RSVD_TP	defin			-9310.37	6631.69			
BL8	VSS	dun		·	7593.33	6682.49			
BM11	VSS	ner		ed u.	6763.51	7022.85			
BM14	vss			1efine	6119.37	7022.85			
BM16	202 202		eined	unos	5475.22	7022.85 7022.85 7022.85	nder		
	202		ed undefined	I	Datasheet, '	Volume 1 of 2			
	d under.	undefin			define				
sine				<u>ي</u> ١٢	1-				



Table 9-2.

	4 under.		ndef	in		16
	U/U-Quad Core/YProcessor BallInform	nation	defined undef		(ir	ntel)
. 6	Table 9-2. Y-Processor Ball				ed une	
Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]
BM18	vss			ed the	4831.08	7022.85
BM20	VSS		24		4186.94	7022.85
BM22	DDR1_DQSN[5] / DDR1_DQSN[3]		DDR1_DQSN[5]	DDR1_DQSN[3]	3542.79	7022.85
	DDR1_DQ[40] / DDR1_DQ[24]		DDR1_DQ[40]	DDR1_DQ[24]	2898.65	7022.85
BM26	DDR1_DQSP[4] / DDR1_DQSP[2]		DDR1_DQSP[4]	DDR1_DQSP[2]	2254.5	7022.85
	DDR1_DQ[32] / DDR1_DQ[16]	y ur	DDR1_DQ[32]	DDR1_DQ[16]	1610.36	7022.85
	DDR1_CS#[0]	sineu			966.22	7022.85
	DDR1_MA[6] /DDR1_CAA[2] /DDR1_MA[6]	DDR1 CAA[2]			322.07	7022.85
O.	DDR1_MA[15] /DDR1_CAA[8]/DDR1_ACT#	DDR1_CAA[8]		inde	-322.07	7022.85
BM36	DDR1_CKP[0]			edu	-966.22	7022.85
	Vss		4	sill"	-1610.36	
	DDR0_DQSN[7] / DDR1_DQSN[5]		DDR0_DQSN[7]	DDR1_DQSN[5]	-2254.5	7022.85
	DDR0_DQ[56] / DDR1_DQ[40]		DDR0_DQ[56]	DDR1_DQ[40]	-2898.65	
BM44	DDR0_DQSP[6] / DDR1_DQSP[4]		DDR0_DQSP[6]	DDR1_DQSP[4]		7022.85
	DDR0_DQ[49] / DDR1_DQ[33]	20	DDR0_DQ[49]	DDR1_DQ[33]		7022.85
	DDR1_DQ[31] / DDR0_DQ[63]	^O sin ^e O	DDR1_DQ[31]	DDR0_DQ[63]	10.	7022.85
BM50	DDR1_DQSP[3] / DDR0_DQSP[7]	deil.	DDR1_DQSP[3]	DDR0_DQSP[7]		7022.85
0	DDR1_DQ[22] / DDR0_DQ[54]	June	DDR1_DQ[22]	DDR0_DQ[54]		7022.85
	DDR1_DQ[22] / DDR0_DQ[34]		DDR1_DQ[22]	DDR0_DQ[54]		7022.85
			DDRI_DQSN[2]			
BM56	DDR0_PAR				-7407.66	
BM59	DDR0_MA[10] /DDR0_CAB[7]/ DDR0_MA[10]	DDR0_CAB[7]	med u			6923.28
BN1	TP4		der.		9310.37	7086.35
	SLP_SUS#		NL		7085.58	7269.23
	RTCRST#	tinet			6441.44	7269.23
. N	DSW_PWROK	der			5797.3	7269.23
NO.	PROC_POPIRCOMP	2 UN		unos	5153.15	7269.23
	RTCX1	0		ed	4509.01	7269.23
BN21	DDR1_DQ[42] / DDR1_DQ[26]		DDR1_DQ[42]	DDR1_DQ[26]	3864.86	7269.23
BN23	DDR1_DQ[45] / DDR1_DQ[29]		DDR1_DQ[45]	DDR1_DQ[29]	3220.72	7269.23
	DDR1_DQ[36] / DDR1_DQ[20]		DDR1_DQ[36]	DDR1_DQ[20]	2576.58	7269.23
BN27	DDR1_DQ[33] / DDR1_DQ[17]		DDR1_DQ[33]	DDR1_DQ[17]	1932.43	7269.23
BN29	VSS	A	Un		1288.29	7269.23
BN3	RSVD	sinel	ſ		8881.11	7111.75
BN31	DDR1_MA[9] /DDR1_CAA[1] /DDR1_MA[9]	DDR1_CAA[1]			644.14	7269.23
BN33	DDR1_CKE[0]	dun.		ion, no	0	7269.23
BN35	DDR1_MA[14] /DDR1_CAA[9]/ DDR1_BG[1]			ed v	-644.14	7269.23
	DDR1_BA[2] /DDR1_CAA[5]/ DDR1_BG[0]	DDR1_CAA[5]		1efin-	-1288.29	7269.23
	DDR0_DQ[59] / DDR1_DQ[43]	ned undefine	DDR0_DQ[59]	DDR1_DQ[43]	etined	d
	undefine	od undern.		- inf	lefines	



Ball # BN4 GPF BN41 DDF BN43 DDF BN43 DDF BN43 DDF BN47 DDF BN47 DDF BN47 DDF BN49 DDF BN53 DDF BN53 DDF BN53 DDF BN53 DDF BN54 VDF BN64 VDF	able 9-2. Y-Processor Ball L Ball Name P_A16 / SD_1P8_SEL R0_DQ[57] / DDR1_DQ[41] R0_DQ[52] / DDR1_DQ[36] R0_DQ[48] / DDR1_DQ[32] R_VTT_CNTL R1_DQ[28] / DDR0_DQ[60] R1_DQ[29] / DDR0_DQ[61] R1_DQ[20] / DDR0_DQ[52] R0_MA[1] /DDR0_CAB[8]/DDR0_MA[1] S R0_ODT[0] R0_BA[0] /DDR0_CAB[4]/DDR0_BA[0]	LIPDDR3	ndefili	V-Quad Core/YProc Non-Interleaved (NIL) DDR1_DQ[41] DDR1_DQ[36] DDR1_DQ[32] DDR0_DQ[60] DDR0_DQ[61] DDR0_DQ[53]	x [um] 8451.85 -2576.58 -3220.72 -3864.86 -4509.01 -5153.15	Y [um] 7111.75 7269.23 7269.23 7269.23 7269.23 7269.23 7269.23 7269.23 7269.23
Ball # BN4 GPF BN41 DDF BN43 DDF BN43 DDF BN47 DDF BN47 DDF BN49 DDF BN53 DDF BN53 DDF BN53 DDF BN53 DDF BN53 DDF BN53 DDF BN54 DDF BN64 VDF BN8 GPF	able 9-2. Y-Processor Ball L Ball Name P_A16 / SD_1P8_SEL R0_DQ[57] / DDR1_DQ[41] R0_DQ[57] / DDR1_DQ[36] R0_DQ[52] / DDR1_DQ[36] R0_DQ[48] / DDR1_DQ[32] R_VTT_CNTL R1_DQ[28] / DDR0_DQ[60] R1_DQ[29] / DDR0_DQ[61] R1_DQ[20] / DDR0_DQ[52] R0_MA[1] /DDR0_CAB[8]/DDR0_MA[1] S R0_ODT[0]	LPDDR3	of 40) Interleaved (IL) DDR0_DQ[57] DDR0_DQ[52] DDR0_DQ[48] DDR1_DQ[28] DDR1_DQ[29] DDR1_DQ[21]	Non-Interleaved (NIL) DDR1_DQ[41] DDR1_DQ[36] DDR1_DQ[32] DDR0_DQ[60] DDR0_DQ[61]	X [um] 8451.85 -2576.58 -3220.72 -3864.86 -4509.01	Y [um] 7111.75 7269.23 7269.23 7269.23
Ball # BN4 GPF BN41 DDF BN43 DDF BN43 DDF BN47 DDF BN47 DDF BN49 DDF BN53 DDF BN53 DDF BN53 DDF BN53 DDF BN53 DDF BN53 DDF BN54 DDF BN64 VDF BN8 GPF	able 9-2. Y-Processor Ball L Ball Name P_A16 / SD_1P8_SEL R0_DQ[57] / DDR1_DQ[41] R0_DQ[57] / DDR1_DQ[36] R0_DQ[52] / DDR1_DQ[36] R0_DQ[48] / DDR1_DQ[32] R_VTT_CNTL R1_DQ[28] / DDR0_DQ[60] R1_DQ[29] / DDR0_DQ[61] R1_DQ[20] / DDR0_DQ[52] R0_MA[1] /DDR0_CAB[8]/DDR0_MA[1] S R0_ODT[0]	LPDDR3	Interleaved (IL) DDR0_DQ[57] DDR0_DQ[52] DDR0_DQ[48] DDR1_DQ[28] DDR1_DQ[29] DDR1_DQ[21]	(NIL) DDR1_DQ[41] DDR1_DQ[36] DDR1_DQ[32] DDR0_DQ[60] DDR0_DQ[61]	8451.85 -2576.58 -3220.72 -3864.86 -4509.01	7111.75 7269.23 7269.23 7269.23
Ball # BN4 GPF BN41 DDF BN43 DDF BN43 DDF BN47 DDF BN47 DDF BN49 DDF BN53 DDF BN53 DDF BN53 DDF BN53 DDF BN53 DDF BN53 DDF BN54 DDF BN64 VDF BN8 GPF	able 9-2. Y-Processor Ball L Ball Name P_A16 / SD_1P8_SEL R0_DQ[57] / DDR1_DQ[41] R0_DQ[57] / DDR1_DQ[36] R0_DQ[52] / DDR1_DQ[36] R0_DQ[48] / DDR1_DQ[32] R_VTT_CNTL R1_DQ[28] / DDR0_DQ[60] R1_DQ[29] / DDR0_DQ[61] R1_DQ[20] / DDR0_DQ[52] R0_MA[1] /DDR0_CAB[8]/DDR0_MA[1] S R0_ODT[0]	LPDDR3	Interleaved (IL) DDR0_DQ[57] DDR0_DQ[52] DDR0_DQ[48] DDR1_DQ[28] DDR1_DQ[29] DDR1_DQ[21]	(NIL) DDR1_DQ[41] DDR1_DQ[36] DDR1_DQ[32] DDR0_DQ[60] DDR0_DQ[61]	8451.85 -2576.58 -3220.72 -3864.86 -4509.01	7111.75 7269.23 7269.23 7269.23
Ball #BN4GPFBN41DDFBN43DDFBN45DDFBN47DDFBN47DDFBN53DDFBN53DDFBN54DDFBN55DDFBN58DDFBN61DDFBN62DDFBN86GPF	Ball Name P_A16 / SD_1P8_SEL R0_DQ[57] / DDR1_DQ[41] R0_DQ[52] / DDR1_DQ[36] R0_DQ[48] / DDR1_DQ[32] R_VTT_CNTL R1_DQ[28] / DDR0_DQ[60] R1_DQ[29] / DDR0_DQ[61] R1_DQ[21] / DDR0_DQ[52] R0_MA[1] /DDR0_CAB[8]/DDR0_MA[1] S R0_ODT[0]	LPDDR3	Interleaved (IL) DDR0_DQ[57] DDR0_DQ[52] DDR0_DQ[48] DDR1_DQ[28] DDR1_DQ[29] DDR1_DQ[21]	(NIL) DDR1_DQ[41] DDR1_DQ[36] DDR1_DQ[32] DDR0_DQ[60] DDR0_DQ[61]	8451.85 -2576.58 -3220.72 -3864.86 -4509.01	7111.75 7269.23 7269.23 7269.23
BN4 GPF BN41 DDF BN43 DDF BN43 DDF BN47 DDF BN47 DDF BN47 DDF BN47 DDF BN53 DDF BN53 DDF BN58 DDF BN61 DDF BN62 DDF BN86 GPF	P_A16 / SD_1P8_SEL R0_DQ[57] / DDR1_DQ[41] R0_DQ[52] / DDR1_DQ[36] R0_DQ[48] / DDR1_DQ[32] R_VTT_CNTL R1_DQ[28] / DDR0_DQ[60] R1_DQ[29] / DDR0_DQ[61] R1_DQ[21] / DDR0_DQ[53] R1_DQ[20] / DDR0_DQ[52] R0_MA[1] /DDR0_CAB[8]/DDR0_MA[1] S R0_ODT[0]	undefined	DDR0_DQ[57] DDR0_DQ[52] DDR0_DQ[48] DDR1_DQ[28] DDR1_DQ[29] DDR1_DQ[21]	(NIL) DDR1_DQ[41] DDR1_DQ[36] DDR1_DQ[32] DDR0_DQ[60] DDR0_DQ[61]	8451.85 -2576.58 -3220.72 -3864.86 -4509.01	7111.75 7269.23 7269.23 7269.23
BN41 DDF BN43 DDF BN45 DDF BN47 DDF BN47 DDF BN47 DDF BN47 DDF BN47 DDF BN51 DDF BN53 DDF BN54 DDF BN55 DDF BN64 VSS BN61 DDF BN62 DDF BN84 GPF	R0_DQ[57] / DDR1_DQ[41] R0_DQ[52] / DDR1_DQ[36] R0_DQ[48] / DDR1_DQ[32] R_VTT_CNTL R1_DQ[28] / DDR0_DQ[60] R1_DQ[29] / DDR0_DQ[61] R1_DQ[21] / DDR0_DQ[53] R1_DQ[20] / DDR0_DQ[52] R0_MA[1] /DDR0_CAB[8]/DDR0_MA[1] S R0_ODT[0]	DDR0_CAB[8]	DDR0_DQ[52] DDR0_DQ[48] DDR1_DQ[28] DDR1_DQ[29] DDR1_DQ[21]	DDR1_DQ[41] DDR1_DQ[36] DDR1_DQ[32] DDR0_DQ[60] DDR0_DQ[61]	-2576.58 -3220.72 -3864.86 -4509.01	7269.23 7269.23 7269.23
BN41 DDF BN43 DDF BN45 DDF BN47 DDF BN47 DDF BN47 DDF BN47 DDF BN47 DDF BN51 DDF BN53 DDF BN54 DDF BN55 DDF BN64 VSS BN61 DDF BN62 DDF BN84 GPF	R0_DQ[57] / DDR1_DQ[41] R0_DQ[52] / DDR1_DQ[36] R0_DQ[48] / DDR1_DQ[32] R_VTT_CNTL R1_DQ[28] / DDR0_DQ[60] R1_DQ[29] / DDR0_DQ[61] R1_DQ[21] / DDR0_DQ[53] R1_DQ[20] / DDR0_DQ[52] R0_MA[1] /DDR0_CAB[8]/DDR0_MA[1] S R0_ODT[0]	DDR0_CAB[8]	DDR0_DQ[52] DDR0_DQ[48] DDR1_DQ[28] DDR1_DQ[29] DDR1_DQ[21]	DDR1_DQ[36] DDR1_DQ[32] DDR0_DQ[60] DDR0_DQ[61]	-2576.58 -3220.72 -3864.86 -4509.01	7269.23 7269.23 7269.23
BN43 DDF BN45 DDF BN47 DDF BN49 DDF BN51 DDF BN53 DDF BN54 DDF BN53 DDF BN54 DDF BN55 DDF BN64 DDF BN61 DDF BN62 DDF BN86 GPF	R0_DQ[52] / DDR1_DQ[36] R0_DQ[48] / DDR1_DQ[32] R_VTT_CNTL R1_DQ[28] / DDR0_DQ[60] R1_DQ[29] / DDR0_DQ[61] R1_DQ[21] / DDR0_DQ[53] R1_DQ[20] / DDR0_DQ[52] R0_MA[1] /DDR0_CAB[8]/DDR0_MA[1] S R0_ODT[0]	DDR0_CAB[8]	DDR0_DQ[52] DDR0_DQ[48] DDR1_DQ[28] DDR1_DQ[29] DDR1_DQ[21]	DDR1_DQ[36] DDR1_DQ[32] DDR0_DQ[60] DDR0_DQ[61]	-3220.72 -3864.86 -4509.01	7269.23 7269.23
BN45 DDF BN47 DDF BN47 DDF BN51 DDF BN53 DDF BN53 DDF BN55 DDF BN56 DDF BN61 DDF BN62 DDF BN86 GPF	R0_DQ[48] / DDR1_DQ[32] R_VTT_CNTL R1_DQ[28] / DDR0_DQ[60] R1_DQ[29] / DDR0_DQ[61] R1_DQ[21] / DDR0_DQ[53] R1_DQ[20] / DDR0_DQ[52] R0_MA[1] /DDR0_CAB[8]/DDR0_MA[1] S R0_ODT[0]	DDR0_CAB[8]	DDR0_DQ[48] DDR1_DQ[28] DDR1_DQ[29] DDR1_DQ[21]	DDR1_DQ[32] DDR0_DQ[60] DDR0_DQ[61]	-3864.86 -4509.01	7269.23
BN47DDFBN49DDFBN51DDFBN53DDFBN55DDFBN58DDFBN61DDFBN62DDFBN64VDEBN8GPF	R_VTT_CNTL R1_DQ[28] / DDR0_DQ[60] R1_DQ[29] / DDR0_DQ[61] R1_DQ[21] / DDR0_DQ[53] R1_DQ[20] / DDR0_DQ[52] R0_MA[1] /DDR0_CAB[8]/DDR0_MA[1] S R0_ODT[0]	DDR0_CAB[8]	DDR1_DQ[28] DDR1_DQ[29] DDR1_DQ[21]	DDR0_DQ[60] DDR0_DQ[61]	-4509.01	
BN49 DDF BN51 DDF BN53 DDF BN55 DDF BN58 DDF BN64 VSS BN61 DDF BN64 VDF BN64 QDF BN64 QDF	R1_DQ[28] / DDR0_DQ[60] R1_DQ[29] / DDR0_DQ[61] R1_DQ[21] / DDR0_DQ[53] R1_DQ[20] / DDR0_DQ[52] R0_MA[1] /DDR0_CAB[8]/DDR0_MA[1] S R0_ODT[0]	DDR0_CAB[8]	DDR1_DQ[29] DDR1_DQ[21]	DDR0_DQ[61]		7269.23
BN51 DDF BN53 DDF BN55 DDF BN58 DDF BN64 VSS BN61 DDF BN62 DDF BN64 VDD BN86 GPF	R1_DQ[29] / DDR0_DQ[61] R1_DQ[21] / DDR0_DQ[53] R1_DQ[20] / DDR0_DQ[52] R0_MA[1] /DDR0_CAB[8]/DDR0_MA[1] S R0_ODT[0]	DDR0_CAB[8]	DDR1_DQ[29] DDR1_DQ[21]	DDR0_DQ[61]	-5153.15	7260.00
BN53 DDF BN55 DDF BN58 DDF BN6 VSS BN61 DDF BN62 DDF BN64 VDE BN86 GPF	R1_DQ[21] / DDR0_DQ[53] R1_DQ[20] / DDR0_DQ[52] R0_MA[1] /DDR0_CAB[8]/DDR0_MA[1] S R0_ODT[0]	DDR0_CAB[8]	DDR1_DQ[21]			
BN55DDFBN58DDFBN6VSSBN61DDFBN62DDFBN64VDEBN8GPF	R1_DQ[20] / DDR0_DQ[52] R0_MA[1] /DDR0_CAB[8]/DDR0_MA[1] S R0_ODT[0]	DDR0_CAB[8]		DUK0_DQ[53] 🔬 🔊	-5797.3	7269.23
BN58 DDF BN6 VSS BN61 DDF BN62 DDF BN64 VDD BN8 GPF	R0_MA[1] /DDR0_CAB[8]/DDR0_MA[1] S R0_ODT[0]	DDR0_CAB[8]	DDR1_DQ[20]	<u></u>	-6441.44	
BN61 VSS BN61 DDF BN62 DDF BN64 VDF BN88 GPF	S R0_ODT[0]	DDR0_CAB[8]		DDR0_DQ[52]	-7085.58	7269.23
BN61 DDF BN62 DDF BN64 VDE BN8 GPF	R0_ODT[0]			sine	-7777.48	7178.04
BN62 DDF BN64 VDE BN8 GPF				ye.	8022.59	7111.75
BN64 VDI BN8 GPF			du.		-8451.85	7111.75
BN8 GPP	R0_BA[0]/DDR0_CAB[4]/DDR0_BA[0]	DDR0_CAB[4]	sine		-8881.11	7111.75
			nde		-9310.37	7086.35
BP1 VS5	P_A6 / SERIRQ	60	0.		7593.33	7111.75
	S	efine			9310.37	7541.01
BP11 SLP	P_LAN#	inoc		-96	6763.51	7541.01
BP14 PCH	H_PWROK	0		Jun	6119.37	7541.01
BP16 PCH	H_OPIRCOMP			sineu	5475.22	7541.01
BP18 RTC	CX2			9er.	4831.08	7541.01
BP20 DRA	AM_RESET#		du		4186.94	7541.01
BP22 VSS	s		sines		3542.79	7541.01
BP24 VD	DQ		nde		2898.65	7541.01
BP26 VD	DQ		10.		2254.5	7541.01
BP28 VSS	s e	fine			1610.36	7541.01
BP3 RSV	VD	noe		6	8855.71	7541.01
BP30 VSS	S	ed v		, uno	966.22	7541.01
BP32 VDI	DQ			cin ^{eo}	322.07	7541.01
BP34 VD	DQ			~9e1.	-322.07	7541.01 7541.01 7541.01 7541.01
BP36 VSS	s		14		-966.22	7541.01
BP38 VSS	s retition		fineo		-1610.36	7541.01
BP40 VDI	DQ UNC		der		-2254.5	7541.01
BP42 VD	DQ	_	6. <i>41</i> ,		-2898.65	7541.01
BP44 VSS	s letti	-sine			-3542.79	7541.01
BP46 VSS	S	nder.			-4186.94	7541.01
BP48 VDI		d'un		nu .	-4831.08	7541.01
		10-		ed v	8401.05	
BP50 VD				1117	-5475.22	7541.01
BP52 VSS	s co		<u>م</u>	UNO-	-6119.37	7541.01
2, 32 , 30	04 Undefined undefine		ed undefined	~		7541.01 7541.01 7541.01
	d une		nder.			
20	04		dui	E	atasheet, V	Volume 1 of 2
	Yell.	213			e	
1						



	undefilite		def	Inec			efined
	U/U-Quad Core/YProcessor BallInform	nation	ndefined undef		(ir	ntel	
	atined t				d und		
- uno	Table 9-2. Y-Processor Ball	List (Sheet 2	7 of 40)	fin	30.		
Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]	
BP54	VSS			aneo	-6763.51	7541.01	
BP56	VDDQ		-96		-7407.66	7541.01	Sine
BP58	VDDQ		dun		-7946.39	7541.01	
BP60	VSS		sino		-8401.05	7541.01	
BP62	VSS		000		-8855.71	7541.01	
BP64	VDDQ	, d (-9310.37	7541.01	
BP7	GPP_A5 / LFRAME# / ESPI_CS#	stine			7946.39	7541.01	
BP9	WAKE#	Inde		Yeu	7407.66	7541.01	
C11	GPP_E13 / DDPB_HPD0			1 Une	6763.51	-7022.85	
C14	VSS			sin ^{eo}	6119.37	-7022.85	
C16	USB3_1_RXN		6	e	5475.22	-7022.85	
C18	USB3_3_RXN		2 Un		4831.08	-7022.85	
C20	PCIE1_RXN / USB3_5_RXN		sinet		4186.94	-7022.85	
C22	PCIE3_RXN		der		3542.79	-7022.85	
C24	PCIE5_RXN	6	0		2898.65	-7022.85	
C26	PCIE7_RXN / SATA0_RXN	fine			2254.5	-7022.85	
C28	PCIE9_RXN	nde		Jeri	1610.36	-7022.85	
C30	CSI2_DN6	ð í		, unc	966.22	-7022.85	
C32	CSI2_DN5			cin ^{eo}	322.07	-7022.85	
C34	CSI2_CLKN2			le''	-322.07	-7022.85	113
C36	CSI2_DN9		2 UN		-966.22	-7022.85	ude.
C38	CSI2_DN11		sines		-1610.36	-7022.85	
C40	vss		"dell		-2254.5	-7022.85	
C42	DDI2_TXP[0]	Ś			-2898.65	-7022.85	
C44	DDI2_TXP[1]	fine			-3542.79	-7022.85	
C46	DDI1_TXP[0]	inde		فعر	-4186.94	-7022.85	
C48	DDI1_TXN[1]	0		, unc	-4831.08	-7022.85	
C50	PCH_JTAG_TDI			in CO	-5475.22	-7022.85	
C52	PCH_TRST#			de1.	-6119.37	-7022.85	undef
C54	PROC_TDI		AUT		-6763.51	-7022.85	
C56	CFG[6]		finer		-7403.09	-7022.85	V
C59	PROC_TMS		.nde.		-8110.22	-6918.2	
D1	vss		0		9310.37	-6631.69	
D10	VSS	fine	-		7085.58	-6776.47	
D12	CL_DATA	inde		کم	6441.44	-6776.47	
D15	USB3_2_RXP / SSIC_RXP	20			5797.3	-6776.47	
D17	USB3_4_RXP			cin ^{eo}	5153.15	-6776.47	
D19	PCIE2_RXP / USB3_6_RXP			defini	4509.01	-6776.47	
D21	PCIE4_RXP		20	<u></u>	3864.86	-6776.47	
	Datasheet, Volume 1 of 2	nia	ed undefined t		ed	underine ² 205	Junde
	undefine	d under.		inc	efine		



	(intel) red undefine			atinet		defin	,ed
	inter ted us		ed unc	U-Quad Core/YProd	nonan Pal		
			Jefine 0/	U-Quad Core/ 1Prod	cessor Bail	Information	
			INOC			Je ₁₁ .	
. In	Table 9-2. Y-Processor Ball	List (Sheet 28	8 of 40)		ned un		
Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]	
D23	PCIE6_RXP			cin ^{eo}	3220.72	-6776.47	
D25	PCIE8_RXP / SATA1A_RXP		6	e	2576.58	-6776.47	<u>U</u> 6
D27	PCIE10_RXP		d un		1932.43	-6776.47	
D29	CSI2_DN4		sinol		1288.29	-6776.47	
D3	eDP_VDDEN		vge,		8881.11	-6682.49	
D31	CSI2_CLKN1	6-			644.14	-6776.47	
D33	CSI2_DN7	Aine			0	-6776.47	
D35	CSI2_DN8	nde.		10	-644.14	-6776.47	
D37	CSI2_DN10	Ō.		, unos	-1288.29	-6776.47	
D39	CSI2_CLKN3	/		ed	-1932.43	-6776.47	
D4	eDP_BKLEN			YG,	8451.85	-6682.49	
	DDI2_TXP[2]		, ur		-2576.58	-6776.47	
	DDI2_TXP[3]		09/11		-3220.72	-6776.47	
	DDI1_TXP[2]		- gern		-3864.86	-6776.47	
	DDI1_TXP[3]	2	1 drive		-4509.01	-6776.47	
	RSVD	sinel			-5153.15		
_	PROC_PRDY#	dell		. 6	-5797.3	-6776.47	
	PROC_TCK	- dull'		ind ^k	-6441.44	-6776.47	
	CFG[5]	6,~		ed u.	-7149.08	-6687.57	
	CFG[10]			1 etine	-7724.65	-6756.15	
	VSS			A0.2	8022.59	-6682.49	ŞĹ,
_	CFG[8]		ed .		-8451.85	-6682.49	
	VSS		AGEIL.		-8881.11	-6682.49	
	VCC		J UNC		-9310.37	-6631.69	
	VSS	6	0		7593.33	-6682.49	
	GPP_E3 / CPU_GP0	defin			6763.51	-6530.09	
	VSS	JUNE		6	6119.37		
	VSS	eu		d un.	5475.22	-6530.09	
_	20.			A HINS		6520.09	
	VSS			nor	4831.08	-6530.09	eti
	VSS		ed l		4186.94		
	VSS		define-		3542.79	-6530.09	
	VSS		uno-		2898.65	-6530.09	
	VSS		e ^{ð -}		2254.5	-6530.09	
	VSS	Aefill	-		1610.36	-6530.09	
	VSS	- une			966.22	-6530.09	
	VSS	ne ^O		d ul	322.07	-6530.09	
	VSS			sinet	-322.07	-6530.09	
	VSS			de.	-966.22	-6530.09	20
E38	vss		6	01.	-1610.36	-6530.09	
	206 undefined		ned undefined	I	Datasheet, '	-6530.09 -6530.09 -6530.09 Volume 1 of 2	
	d un.	inde			defini		
				· U			



und^{efined un}

	indefine		Let	ineo -			stined
	U/U-Quad Core/YProcessor BallInform	nation	defined unc		(ir	ntel	37.
	Table 9-2. Y-Processor Ball	List (Sheet 20	9 of 40)		ed unit	2	
Ball #		LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]	
E40	VSS			- ed	-2254.5	-6530.09	2
E42	VSS		26		-2898.65		
E44	VSS		, uno		-3542.79		
E46	VSS		00		-4186.94		
E48	VSS		Der.		-4831.08	-6530.09	
E50	VSS	24	<u>, () </u>		-5475.22		
E52	VSS	sineu.			-6119.37		
E54	VSS			leftif	-6763.51		
E56	VSS			inou	-7509.26		
E59	VSS			ed	-8088.88	-6413.25	
F1	RSVD		~	C, I, I	9310.37	-6177.03	
F10	GPP_E4 / DEVSLP0		1 UNO		7085.58	-6283.71	9e,
F12	CL_CLK		^O 9 _{0 ib}		6441.44	-6283.71	
F15	USB3_2_TXN / SSIC_TXN		det.		5797.3	-6283.71	
F17	USB3_4_TXN	2			5153.15	-6283.71	
F19	PCIE2_TXN / USB3_6_TXN	- sine			4509.01	-6283.71	
F21	PCIE4_TXN	ndei		101	3864.86	-6283.71	
F23	PCIE6_TXN	d Ville		, unos	3220.72	-6283.71	
F25	PCIE8_TXN / SATA1A_TXN	· ·		ed	2576.58	-6283.71	
F27	PCIE10_TXN			101	1932.43	-6283.71	nia.
F29	CSI2_DP0		d UN		1288.29	-6283.71	
F3	RSVD		^O 9 _{0is}		8881.11	-6253.23	
F31	CSI2_CLKP0		deil		644.14	-6283.71	
F33	CSI2_DN1	6			0	-6283.71	
F35	CLKOUT_PCIE_P1	fines			-644.14	-6283.71	
F37	CLKOUT_PCIE_P4			20	-1288.29	-6283.71	
F39	CLKOUT_PCIE_P5	0		, uno	-1932.43	-6283.71	
F4	GPP_E21 / DDPC_CTRLDATA	0		the co	8451.85	-6253.23	
F41	DDI1_AUXP			4ethi	-2576.58	-6283.71	
F43	EDP_TXP[3]				-3220.72	-6283.71	Indefin
F45	EDP_TXP[0]		^{Co} nia		-3864.86	-6283.71	
F47	PROC_TRST#		ndeit		-4509.01	-6283.71	
F49	PECI		0		-5153.15	-6283.71	
F51	BPM#[2]	fine			-5797.3	-6283.71	
F53	CFG[1]	inde.		X	-6441.44	-6283.71	
F55	CFG[7]	<u>60</u>			-7085.58	-6283.71	
F6	GPP_E16 / DDPE_HPD3			^O 9nia	8022.59	-6253.23	
F61	CFG[11]			deit	-8477.25	-6253.23	12
F62	VSS		AU		-8881.11	-6253.23	
	Datasheet, Volume 1 of 2	nia.	ed undefined t		ed	-6283.71 -6253.23 -6253.23 -6253.23	
	undefine	ed under		. und	etine		



	(intel) red undefine		-96	stine		in the second	Ine
	ed		d une			inde.	
	(intel)		u/	U-Quad Core/YPro	cessor Ball	Information	
			inde.			efille	
	Aine	ed '			J UN		
	Table 9-2. Y-Processor Ball I	List (Sheet 30) of 40)				
Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]	
564	VCC				-9310.37	-6171.03	
	GPP_E11 / USB2_OC2#			sino	7593.33	-6171.03	
	GPP_E0 / SATAXPCIE0 / SATAGP0		in the second se		6763.51	-6037.33	
	VSS		ed -		6119.37	-6037.33	
-	USB3_1_TXN		Jefil'		5475.22	-6037.33	
	USB3_3_TXN		din .		4831.08	-6037.33	
	PCIE1_TXN / USB3_5_TXN	0.9m			4186.94	-6037.33	
	PCIE3_TXN	delli			3542.79	-6037.33	
20	PCIES_TXN			inde	2898.65	-6037.33	
	PCIES_TXN / SATA0_TXN			ed u.	2254.5	-6037.33	
	PCIE9_TXN			410°	1610.36	-6037.33	
	CSI2_DP2		<u></u>	0	966.22	-6037.33	e,
	CSI2_DP3				322.07	-6037.33	
	CLKOUT_ITPXDP_P		Jefin .		-322.07	-6037.33	
	CLKOUT_PCIE_P2	2	U.N.		-966.22	-6037.33	
	CLKOUT_PCIE_P3	inel .) 		-1610.36		
	DDI2_AUXP	delli			-2254.5	-6037.33	
0	EDP_AUXP	à un		nd ^e	-2898.65		
~	EDP_TXP[1]	87		ed	-3542.79	-6037.33	
	EDP_TXP[2]			16/1/1	-4186.94		
	PROC_TDO			A0	-4831.08		
	BPM#[3]		eo -		-5475.22		
	CFG[0]		- defin		-6119.37		
	CFG[17]		dun		-6763.51	-6037.33	
	CFG[18]	eine sine			-7417.82		
	CFG[9]	ndell			-7818.63		
0	GPP_E5 / DEVSLP1	o un		nu inc	7170.42	5000.04	
H12	RSVD			ed	6441.44	-5790.95	
H15	USB3_2_TXP / SSIC_TXP			Ye	5797.3	-5790.95	
	USB3_4_TXP	1	21	100	5153.15	-5790.95	de
	PCIE2_TXP / USB3_6_TXP		sinco		4509.01	-5790.95	÷ ۳
	SYS_RESET#	1	. de.	1	9038.59	-5797.3	
H21	PCIE4_TXP	1	0,01,	1	3864.86	-5790.95	
H23	PCIE6_TXP	γ_{ij}	e	1	3220.72	-5790.95	
H25	PCIE8_TXP / SATA1A_TXP	nde			2576.58	-5790.95	
H27	PCIE10_TXP	ed		, un	1932.43	-5790.95	
H29	CSI2_DN0			. ned	1288.29	-5790.95	
H31	CSI2_CLKN0	1		den	644.14	-5790.95	
H33	CSI2_DP1			une	0	-5790.95	6,
	208 undefined undefine	1	ned undefined		Datasheet, '	-5790.95 -5790.95 -5790.95 Volume 1 of 2	
	d ur.	INOS			det		
				10 . U	70-		



	unden.		ndef	Ine		de
	U/U-Quad Core/YProcessor BallInform	nation	Idefined undef		(ír	itel
	ned U.	y ur	10-			
- 26	Table 9-2.Y-Processor Ball	l ist (Sheet 3	1 of 40)		du.	
un		no		Non-Interleaved		
Ball #	Ball Name	LPDDR3	Interleaved (IL)	(NIL)	X [um]	Y [um]
H35	CLKOUT_PCIE_N1			aner	-644.14	-5790.95
	CLKOUT_PCIE_N4		nde		-1288.29	
	CLKOUT_PCIE_N5		du.		-1932.43	-5790.95
	GPP_E20 / DDPC_CTRLCLK		atine		8545.83	-5797.3
	DDI1_AUXN		000		-2576.58	
	EDP_TXN[3]	ed '	P		-3220.72	
	EDP_TXN[0]	efine			-3864.86	
0	THERMTRIP#	Inos		dell	-4509.01	
_	CATERR#			dulli	-5153.15	
	BPM#[0]			sinec	-5797.3	-5790.95
	CFG[3]		60.	61	-6441.44	
	CFG[4]		d v.		-7085.58	
	CFG[15]		stine		-8130.79	
	GPP_E19 / DDPB_CTRLDATA		MOG		8053.07	-5797.3
	CFG[14]	ed	<u> </u>		-8545.83	
	VCC	Jefil'			-9038.59	
~O	GPP_E8 / SATALED#	une		der	7560.31	-5797.3
	SYS_PWROK			d UI.	9310.37	-5475.22
	GPP_E1 / SATAXPCIE1 / SATAGP1			AINES	6763.51	-5544.57
	VSS			Se.	6119.37	-5544.57
	USB3_1_TXP		ed V.		5475.22	-5544.57
	USB3_3_TXP		1efine		4831.08	-5544.57
	PCIE1_TXP / USB3_5_TXP		inos		4186.94	-5544.57
	PCIE3_TXP	ec			3542.79	-5544.57
	PCIE5_TXP	defin.			2898.65	-5544.57
0	PCIE7_TXP / SATA0_TXP	a une		de	2254.5	-5544.57
	PCIE9_TXP VSS	20		dui	1610.36	-5544.57
				nine in the second	8792.21	-5475.22
	CSI2_DN2 CSI2_DN3			05	966.22 322.07	-5544.57 -5475.22 -5544.57 -5544.57
	CSI2_DN3 CLKOUT_ITPXDP_N		ed v		-322.07	-5544.57
	CLKOUT_PCIE_N2		- Lefill'		-966.22	-5544.57
	CLKOUT_PCIE_N2		1 UNV		-1610.36	76.
	DDI2_AUXN	A CO	0		-2254.5	-5544.57
	EDP_AUXN	ade ^[]			-2898.65	
	EDP_TXN[1]	Julie		bn,	-3542.79	
				ed u.	-4186.94	-5544.57
	PROCHOT#			10 refine	-4831.08	-5544.57
				20-	8299.45	-5475.22
12	A STINGS		ed undefined u			
	4 UNO-		ndein			unde 109
	Datasheet, Volume 1 of 2		dui.			209
	undefine					
					7113	



Table 9-2.

	(intel) red undefine		h	3411-		.efi	'Jec
			and un	U-Quad Core/YProd	ressor Ball	Information	
	(inter		defill			fine	
		21	nuc.		n,		
	Table 9-2. Y-Processor Ball	List (Sheet 32	2 of 40)		ed u.		
Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]	
150	BPM#[1]	0			-5475.22	-5544.57	
	CFG[2]			sino	-6119.37	-5544.57	
	CFG[16]				-6763.51	-5544.57	
	CFG[19]		ed		-7407.66	-5544.57	
	CFG[13]		- delli.		-7805.93	-5605.53	
	CFG[12]		Jan.		-8299.45		
	VSS	0.90	<u>}</u>		-8792.21	-5475.22	
	VCC	dell.			-9310.37	-5475.22	
20	VSS	June		inde	7806.69	-5475.22	
	VSS	S.		ed U.	7313.93	-5475.22	
	RSVD			1 Still	6441.44	-5298.19	
	VSS		90.	0.0	5797.3	-5298.19	
	VSS		ed		5153.15	-5298.19	
	VSS		Jefli.		4509.01	-5298.19	
	VSS		<u>n hilo.</u>		3864.86	-5298.19	
	VSS	- inel			3220.72	-5298.19	
	VSS	dell.			2576.58	-5298.19	
	VSS	June		nd ^k	1932.43	-5298.19	
	VSS	C. C		ed V.	1288.29	-5298.19	
	VSS			in cinc	644.14	-5298.19	
	VSS			200	044.14	-5298.19	e,
	VSS		ed .		-644.14	-5298.19	
	VSS		Actil.		-1288.29	-5298.19	
	VSS		June		-1932.43	-5298.19	
	VSS		20		-2576.58	-5298.19	
	VSS	dell'			-3220.72	-5298.19	
	VSS	June		Ind	-3864.86		
	23/	in ev		ed v.	-4509.01	-5298.19	
	VSS			16111	-5153.15	-5298.19	
	VSS			10 ⁻	-5797.3	-5298.19 -5298.19 -5298.19 -5298.19	
	VSS		fined		-6441.44	-5298.19	
	VSS		detti.		-7085.58	-5298.19	
	GPP_E14 / DDPC_HPD1		A un		7067.55	-5153.15	
	VSS	275	(e		6119.37	-5051.81	
	RSVD	-dell'			5475.22	-5051.81	
	RSVD	-d ull'		n	4831.08	-5051.81	
	XTAL24 OUT	NPC-		edv	9038.59	-5153.15	
	RSVD			26111-	4186.94	-5051.81	
1.2.2			<u>.</u>	UN ^{O-}	3542.79	-5051.81	.96
LI	210 210 a undefined undefined	ja.	ned undefined	1	Datasheet, V	-5051.81 -5051.81 -5051.81 Volume 1 of 2	ь."
	d un-	ude.			definit		
		du.		1.	Jr.		



Table 9-2.

Inoc		Jef	Ineo			sined u
U/U-Quad Core/YProcessor BallInform	nation	defined unc		(ir	itel	(e.,
Table 9-2. Y-Processor Ball	List (Sheet 33	3 of 40)		d une		
Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]	
RSVD			Loed Children	2898.65	-5051.81	2
		20				
		, unu				9e1.
		00		966.22		
		der"				
	20				6	
	sineu			A U'		
	Joe''		e i f			
			Inde			
			ed			2
		2	B S S S S S S S S S S S S S S S S S S S			
		, uno				derr
		CO CO				
		Jein .				
	×	UN ^C				
	sineu			1 V.		
	ole'''		il.			
	<u>d</u>		1000			
			ed			
			eil			Sine
		, un	<u>.</u>			gen
		ineo -				7/1-
		Jefin.				
4		MUC.			20.	
	sineo			<u>, U</u>		
	delli					
	Juli		nde			
	36.		ed v.			
20.			11/2			
V.		in .	0-			undefin
		and a				UI
		detti.				
		A UNY			70.	
	Sine	0				
	voein.					
	10 111		bn.		-4805.43	
VCC	6-		ed v.		-4805.43	
vcc			Jetine Jetine	-1288.29	-4805.43	undefil
		ed undefined u	20 ⁻	-1932.43	-4805.43	dern
	Table 9-2.Y-Processor BallBall NameRSVDRSVDRSVDRSVDVCCSAVCC_SENSERSVDRSVDGPP_E23VCCVCCVCCVCCVCCVCCVCCVCCVCCVCCVCCVCCVCCVCCVCCVCCVSSGPP_E18 / DDPB_CTRLCLKVSSVCCVCCVCCVCCVSSGPP_E6 / DEVSLP2XTAL24_INGPP_E10 / USB2_OC1#RSVD	Bail NameLPDDR3RSVDRSVDRSVDVCCSAVSS_SENSEVCC_SENSERSVDRSVDGPP_E23VCCVCCVCCVCCVCCVCCVCCVCCVCCVCCVCCVCCVCCVCCVCCVCCVSSGPP_E18 / DDPB_CTRLCLKVSSVCCGPP_E10 / USB2_OC1#RSVD <td>Table 9-2. Y-Processor Ball List (Sheet 33 viet) RSVD Interleaved (II) VCCSA Interleaved (II) RSVD Interleaved (II) VCC Interleaved (II) VCC</td> <td>Table 9-2. Y-Processor Ball List (Sheet 3: Joint and the second of the s</td> <td>Table 9-2. Y-Processor Ball List (Sheet 33 J-V)Ball NameLPDDR3Interleaved (L)Mon-Interleavel (L)X (un)RSVDIII2896.65RSVDIII2896.65RSVDIIII1610.36VCCSAIIII1610.36VCCSAIII1610.36322.07VCCSAIII966.22967.23RSVDIII966.22967.23RSVDIII966.23967.23VCCIII1610.36967.23VCCIII1610.36967.23VCCIII1610.36967.23VCCIII1610.36967.23VCCIII1610.36967.23VCCIII1610.36967.23VCCIII1610.36VCCIII1610.36VCCIII1610.36VCCIII1610.36VCCIII1610.36VCCIII1610.36VCCIII1610.36VCCIII1610.36VCCIII1610.36VCCIII1610.36VSSIIII1610.3</td> <td>Solution Solution Solution</td>	Table 9-2. Y-Processor Ball List (Sheet 33 viet) RSVD Interleaved (II) VCCSA Interleaved (II) RSVD Interleaved (II) VCC Interleaved (II) VCC	Table 9-2. Y-Processor Ball List (Sheet 3: Joint and the second of the s	Table 9-2. Y-Processor Ball List (Sheet 33 J-V)Ball NameLPDDR3Interleaved (L)Mon-Interleavel (L)X (un)RSVDIII2896.65RSVDIII2896.65RSVDIIII1610.36VCCSAIIII1610.36VCCSAIII1610.36322.07VCCSAIII966.22967.23RSVDIII966.22967.23RSVDIII966.23967.23VCCIII1610.36967.23VCCIII1610.36967.23VCCIII1610.36967.23VCCIII1610.36967.23VCCIII1610.36967.23VCCIII1610.36967.23VCCIII1610.36VCCIII1610.36VCCIII1610.36VCCIII1610.36VCCIII1610.36VCCIII1610.36VCCIII1610.36VCCIII1610.36VCCIII1610.36VCCIII1610.36VSSIIII1610.3	Solution Solution



Table 9-2.

	(intel) red undefine		- 49	stine			
	ned L.		d unc			inden	
	(Intel)		u/	U-Quad Core/YPro	cessor Ball	Information	
			Inde			lef11.	
	Alle	ed '			d un		
n,	Table 9-2. Y-Processor Ball I	List (Sheet 34	l of 40)		neu		
Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]	
M41	VCC			e de la	-2576.58	-4805.43	
	VCC		2	C'	-3220.72	-4805.43	
	VCC		, uni		-3864.86	-4805.43	
	VCC		^O O _{Ni}		-4509.01	-4805.43	
	VCC		-dell.		-5153.15	-4805.43	
	GPP_E22	λ	40-		8299.45	-4831.08	
	VCC	einev.			-5797.3	-4805.43	
	VCC	ndell		101	-6441.44	-4805.43	
0	VCC	0		1000	-7341.87	-4989.83	
	VCC			ed	-7806.69	-4831.08	
	VCC			A6111	-8299.45	-4831.08	
	VCC		, ur		-8792.21	-4831.08	
	VCC		Conicia Conicia		-9310.37	-4831.08	
	GPP_E15 / DDPD_HPD2		deili		7806.69	-4831.08	
	GPP_E7 / CPU_GP1	2			7313.93	-4831.08	
	GPP_E2 / SATAXPCIE2 / SATAGP2	sine!			7067.55	-4509.01	
	GPP_E9 / USB2_OC0#	ndel.		10	6574.79	-4509.01	
	VSS	0. 11.		inor	6119.37	-4559.05	
	VSS			ed	5475.22	-4559.05	
_	VSS			764111	4831.08	-4559.05	
	USB2_COMP		, 0	<u></u>	9038.59	-4509.01	6,
	VSS		cine0		4186.94	-4559.05	
	VSS		deil.		3542.79	-4559.05	
	VSS		2000		2898.65	-4559.05	
	VSS	sine			2254.5	-4559.05	
N28	VSSSA_SENSE	nde'.			1610.36	-4559.05	
N30	VCCSA	d'un		onu .	966.22	-4559.05	
	vcc			. ned	322.07	-4559.05	
N34	vcc			-96th	-322.07	-4559.05	
	vcc		14	J.C.	-966.22	-4559.05	Jefi
N38	vcc		fineo		-1610.36	-4559.05	
N4	GPP_D4 / FLASHTRIG		gen.		8545.83	-4509.01	
N40	vcc		duin		-2254.5	-4559.05	
N42	vcc	713-	C.		-2898.65	-4559.05	
N44	VCCGT	.nder.			-3542.79	-4559.05	
N46	VCCGT	ed u		nu .	-4186.94	-4559.05	
N48	VCCGT			ed -	-4831.08	-4559.05	
N50	VCCGT			-96th	-5475.22	-4559.05	
N52	VCCGT_SENSE		4	uni	-6119.37	-4559.05	'9 ₆
	212 212	j).	ned undefined		Datasheet, V	-4559.05 -4559.05 -4559.05 Volume 1 of 2	
	d un-	ude.			retitie		
		du.			nu-		



Table 9-2.

Indefine		def	Ined			efined u
U/U-Quad Core/YProcessor BallInfor	mation	defined unc		(ir	itel	27.
Table 9-2. Y-Processor Bal	l List (Sheet 3	5 of 40)		d une		
	LPDDR3	Interleaved (IL)	Non-Interleaved	X [um]	Y [um]	
VCC	·		- ed V	-6777.48	-4586.99	20
		20	in.			
		, uno-				
		ane ⁰				
		- definit				
	~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~	100				
	sineu					
	aden.					
	9.0/		inde	9310.37	-4186.94	
	-		ed t	6821.17	-4186.94	*
		2	C I I I			
		, uno				9e1.
		O O O O O		8299.45	-4186.94	
		'9er,		-6423.66		
	~	400				
	sineu			1 V.		
	ndel.			-7806.69	-4186.94	
	-0-		inde	-8299.45		
	0		ed v	-8792.21	-4186.94	
			C	-9310.37	-4186.94	einel
GPP_D5 / ISH_I2C0_SDA				7806.69	-4186.94	der
GPP_D1		09nia		7313.93	-4186.94	
~O~		odell.		7067.55	-3864.86	
	2			6574.79	-3864.86	
	-sinel	<u>,                                     </u>		5846.1	-4104.91	
	nder		10	5350.8	-4104.91	
	ed un		. unoc	4855.5	-4104.91	
			ed	4360.2	-4104.91	
VSS			2011	9038.59	-3864.86	
2 V.		1 UT		3864.9	-4104.91	undefine
		cin ^{eo}		3369.6	-4104.91	0.
VSS		derr		2874.3	-4104.91	
VCCSTG	_	6 ⁰¹ .		2379	-4104.91	
VCCPLL	-fine			1883.7	-4104.91	
VCCSA	nder		26	1388.4	-4104.91	
VSS	O W		, uno	893.1	-4104.91	
vcc	(C)		ined -	397.8	-4104.91	
			-96till	-97.5	-4104.91	7/3_
VCCG0		ed undefined u		-592.8	-4104.91	undefin
	Table 9-2.         Y-Processor Bal           #         Ball Name           VCC         VCC           VCC         VCC           VCC         VCC           VCC         GPP_D0           VCC         VCC           VCC         VSS           VSSGT_SENSE         VSS           VCC         VCC           VCCAPLLEBB_1P0         VSS           VCCLK5         VSS           VCCCLK5 <t< td=""><td>Ball Name         LPDDR3           VCC        </td><td>Table 9-2.         Y-Processor Ball List (Sheet 35 of 40)           #         Ball Name         LPDDR3         Interleaved (1L)           VCC         -         -         -           GPP_D2         xctx, BIASREF         -         -           GPD5         -         -         -         -           VSS         -         -         -         -           VCC         -         -         -         -           VCC         -         -         -         -           VCC         -         -         &lt;</td><td>Fable 9-2.         Y-Processor Ball List (Sheet 35 of 40)           #         Ball Name         LPDDR3         Interleaved (LL)         Non-Interleaved (KL)           VCC         Image: Constraint of the state of t</td><td>Table 9-2.         Y-Processor Ball List (Sheet 35 of 40)           Rail Name         LPDR3         Interleaved (L)         Non-Interleaved (NIL)         X (Lm)           VCC         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -<td>JU2-Quad Core/PProcessor BallInformation         Interleaved (II)         Non-Interleaved (II)</td></td></t<>	Ball Name         LPDDR3           VCC	Table 9-2.         Y-Processor Ball List (Sheet 35 of 40)           #         Ball Name         LPDDR3         Interleaved (1L)           VCC         -         -         -           GPP_D2         xctx, BIASREF         -         -           GPD5         -         -         -         -           VSS         -         -         -         -           VCC         -         -         -         -           VCC         -         -         -         -           VCC         -         -         <	Fable 9-2.         Y-Processor Ball List (Sheet 35 of 40)           #         Ball Name         LPDDR3         Interleaved (LL)         Non-Interleaved (KL)           VCC         Image: Constraint of the state of t	Table 9-2.         Y-Processor Ball List (Sheet 35 of 40)           Rail Name         LPDR3         Interleaved (L)         Non-Interleaved (NIL)         X (Lm)           VCC         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         - <td>JU2-Quad Core/PProcessor BallInformation         Interleaved (II)         Non-Interleaved (II)</td>	JU2-Quad Core/PProcessor BallInformation         Interleaved (II)         Non-Interleaved (II)



# Table 9-2.

	(intel) red undefine		ndf	Stir.		1991	ver
	(intal) eo		uned un	U-Quad Core/YProd	cessor Ball	Information	
	(inter		defill			sine	
		21	TUC		n, n		
	Table 9-2. Y-Processor Ball I	List (Sheet 36	5 of 40)		ned u.		
Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]	
R36	VSS			ed the	-1088.1	-4104.91	
	VCCG0		2	CIII -	-1583.4	-4104.91	
	VSS		, uni		8545.83	-3864.86	
	VSS		000		-2078.7	-4104.91	
	VCC		-9e(),		-2574	-4104.91	
	VSS	A	400		-3069.3	-4104.91	
	VSS	sineu			-3564.6	-4104.91	
	VSS	dell		0	-4059.9	-4104.91	
20	VSS			inac	-4555.2	-4104.91	
	VSS	/		ed	-5050.5	-4104.91	
_	VSS			16111	-5545.8	-4104.91	
	VCCGT		, ur		-6041.1	-4104.91	<u>}</u>
	VCCGT		ineo -		-6574.79	-3864.86	
	VSS		John .		-7067.55	-3864.86	
	VCC	2			-7560.31	-3864.86	
	VCC	ein ^{el}			-8053.07	-3864.86	
	VSS	dell		10	8053.07	-3864.86	
	VCC	0,000		ind!	-8545.83	-3864.86	
	VCC			ed	-9038.59	-3864.86	
	VSS			26111	7560.31	-3864.86	
	VCCMPHYGT_1P0			<u>0</u> 0-	9310.37	-3542.79	
	GPP_D12		eo -		6821.17	-3542.79	
	VSS		defin		6328.41	-3537.71	
	VCCMPHYGT_1P0		dun		5846.1	-3546.11	
	VCCMPHYGT_1P0	- nis			5350.8	-3546.11	
	VSS	Joe''			4855.5	-3546.11	
	VCCCLK6	-0 ·JII.		in ^o	4360.2		
	VSS			ed	3864.9	-3546.11	
	VSS			76 <u>1</u> 11	3369.6	-3546.11	
	VSS	+	1	<u> </u>	2874.3	-3546.11 -3546.11 -3546.11 -3546.11	
	VCCSTG	+	fineo		2379	-3546.11	
	VCCPLL		deriv		1883.7	-3546.11	
	VCCSA		- A WIN-		1388.4	-3546.11	
	GPP_D8 / ISH_I2C1_SCL	7/13	<u>e</u> ~		8792.21	-3542.79	
	VCCSA	nder			893.1	-3546.11	
	VCC	d'un			397.8	-3546.11	
	VSS			ed	-97.5	-3546.11	
	VCCG0	1		1 ACT I	-592.8	-3546.11	
<b>T</b> 2C		1	<u> </u>	Un	-1088.1	-3546.11	<i>.0</i> ⁶
LI	214 a undefined undefine	Ĭà.	ned undefined		Datasheet, V	-3546.11 -3546.11 -3546.11 /olume 1 of 2	
	dunz	uder			defins		
		du.			70.		



# Table 9-2.

	undefit.		def	ING		i.
	U/U-Quad Core/YProcessor BallInform	ation	defined une		(ir	itel
	afined	tined ut			d une	31.
d uno	Table 9-2. Y-Processor Ball I	List (Sheet 3		Non-Interleaved	30	T]
Ball #	Ball Name	LPDDR3	Interleaved (IL)	(NIL)	X [um]	Y [um]
T38	VCCG0			ineu	-1583.4	-3546.11
T40	vss		nde		-2078.7	-3546.11
T41	VCC		du.		-2574	-3546.11
T43	VCCGT		sine		-3069.3	-3546.11
T44	VCCGT		nde		-3564.6	-3546.11
T46	VCCGT	ed t			-4059.9	-3546.11
T47	VCCGT	efine			-4555.2	-3546.11
T49	VCCGT	una		den	-5050.5	-3546.11
Т5	GPP_D11	ст. 		dun	8299.45	-3542.79
Т50	VCCGT			sinec.	-5545.8	-3546.11
T51	VCCGT		60.	e	-6041.1	-3546.11
T54	VCCGT		d v.		-6821.17	-3542.79
Т56	VSS		stine		-7313.93	
Т58	VSS		Mas		-7806.69	
T60	VSS	ed	0		-8299.45	
T62	VSS	Jefill'			-8792.21	
T64	VSS	uno		der	-9310.37	
Т7	GPP_D10	2		d Un.	7806.69	-3542.79
Т9	GPP_D7 / ISH_I2C1_SDA			- sinc	7313.93	-3542.79
U10	GPP_D13 / ISH_UARTO_RXD / SMLOBDATA		191		7067.55	-3220.72
U12	GPP_D17 / DMIC_CLK1		ed v		6574.79 9038.59	-3220.72
U2	VCCMPHYGT_1P0 GPP_D14 / ISH_UART0_TXD / SML0BCLK		Jeff III			
U4			unor		8545.83 -6574.79	-3220.72 -3220.72
U53	VCCGT	e			-7067.55	~
U55	VCCGT	defili			-7560.31	
U57 U59	VCCGT	June		nd ^e	-8053.07	
U6	GPP_D15 / ISH_UART0_RTS#			ed VI	8053.07	-3220.72
U61	VCCGT			161112	-8545.83	-3220.72
U63	VCCGT			0-	-9038.59	
U8	GPP_D18 / DMIC_DATA1		ed -		7560.31	-3220.72
V1	VCCMPHYAON_1P0	+	detin		9310.37	-2898.65
V1 V11	GPP_D20 / DMIC_DATA0		2 Un		6821.17	-2898.65
V13	VSS	4108	<u> </u>		6328.41	-2893.57
V15	VCCAMPHYPLL_1P0	ndein.			5846.1	-2987.31
V15	VCCAMPHYPLL_1P0	19 m.		ind!	5350.8	-2987.31
V18				ed	4855.5	-2987.31
V19	VCCCLK2			1641115	4360.2	-2987.31
V21	VCCCLK4			0	3864.9	-2987.31
L	Datasheet, Volume 1 of 2	nia.	ed undefined u		od	-2987.31 -2987.31 -2987.31 215
	undefine	d under.		inc	efine	



	(intel) red undefine		d unc			Inde
	(intel)		sine u/	U-Quad Core/YProc	cessor Ball	Information
	1.00-2		inde.			efilie
	Aine	ed			, un	
	Table 9-2. Y-Processor Ball	List (Sheet 38	3 of 40)			
Ball #	Ball Name	UN LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]
V23	VCCCLK3	<i>r</i>			3369.6	-2987.31
	VSS		2	sill ^o	2874.3	-2987.31
	VCCST		, uni		2379	-2987.31
	VSS		000		1883.7	-2987.31
	VCCSA		defin		1388.4	-2987.31
	GPP_D19 / DMIC_CLK0	λ	Jan Star		8792.21	-2898.65
	VSS	einev.			893.1	-2987.31
	VCC	nder.		10	397.8	-2987.31
0	VSS	6. <u></u>		innou	-97.5	-2987.31
	VCCG0	/		ed	-592.8	-2987.31
	VSS			Ye.	-1088.1	-2987.31
	VCCG0	1			-1583.4	-2987.31
	VSS	1	cine0		-2078.7	-2987.31
	VCC		aden.		-2574	-2987.31
V43	VSS		0		-3069.3	-2987.31
V44	VSS	fine			-3564.6	-2987.31
V46	VSS	nder		20	-4059.9	-2987.31
V47	VSS	d'		no-	-4555.2	-2987.31
V49	VSS			rined	-5050.5	-2987.31
V5	GPP_D23 / I2S_MCLK			100 Million	8299.45	-2898.65
V50	VSS		A V		-5545.8	-2987.31
V51	VSS		eine ^c		-6041.1	-2987.31
V54	VCCGT		dell		-6821.17	-2898.65
V56	VCCGT		.6		-7313.93	-2898.65
V58	VCCGT	fine			-7806.69	-2898.65
V60	VCCGT	inde		A	-8299.45	-2898.65
V62	VCCGT	ed th			-8792.21	-2898.65
V64	VCCGT			sinec	-9310.37	-2898.65
V7	GPP_D22			den	7806.69	-2898.65
V9	GPP_D16 / ISH_UART0_CTS# / SML0BALERT#		6	y.	7313.93	-2898.65 -2898.65 -2898.65 -2898.65
	GPP_C7 / SML1DATA	1	onino		7067.55	-2576.58
W12	GPP_D21	1	inde	1	6574.79	-2576.58
W2	VCCMPHYAON_1P0		eb	1	9038.59	-2576.58
W4	GPP_C3 / SMLOCLK	<i>Aetin</i>		1	8545.83	-2576.58
W53	VCCGT	4 UNU		~	-6574.79	-2576.58
W55	VCCGT	heo		-9 ch	-7067.55	-2576.58
W57	VCCGT	1		filler	-7560.31	-2576.58
W59				inde	-8053.07	-2576.58
	216		ned undefined			-2576.58 -2576.58 -2576.58
	unde		defin			stineu
	216		dur	I		Volume 1 of 2
	den		ner		ndefine	
	, un				stine	



	undefill		def	Ineo		i.	ined
	U/U-Quad Core/YProcessor BallInfor	mation	defined une		(ir	tel	
	Table 9-2. Y-Processor Ball	List (Sheet 39	9 of 40)		d une		
Ball		LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]	
W6	GPP_C1 / SMBDATA			(0)	8053.07	-2576.58	
W61			24	100	-8545.83		
W61 W63	<u> </u>		NOC		-9038.59	-2576.58	
W8	GPP_C2 / SMBALERT#		00		7560.31	-2576.58	
Y1	VSS		Aer III		9310.37	-2254.5	
Y11	VSS	20	0		6821.17	-2254.5	
Y13	VSS	sineo			6328.41	-2249.42	
Y15	VSS	odelli		2172	5846.1	-2428.51	
Y16	VSS			inde.	5350.8	-2428.51	
Y18	VCCCLK1	-		ed V	4855.5	-2428.51	
Y19	VCCCLK2		2	2`\`\`` 2``	4360.2	-2428.51	
Y21	VCCCLK4		, uno		3864.9	-2428.51	e,
Y23	VCCCLK3		ed		3369.6	-2428.51	
Y24	VSS		detin.		2874.3	-2428.51	
Y26	VCCST		JAN		2379	-2428.51	
Y20	VSS	0.9nis			1883.7	-2428.51	
Y27	VCCSA	aden.		iii.	1388.4	-2428.51	
Y29	VSS	dulli		uge.	8792.21	-2428.51	
<u></u>	VCCSA	37		ed v.	893.1	-2428.51	
Y30 Y32	VCC			Cilly Cilly	397.8	-2428.51	
Y32 Y33	VSS		in in	<u>}</u>	-97.5	-2428.51	dein'
	VCCG0		ed ~		-592.8	-2428.51	
Y35	VSS		ACTIV-		-1088.1	-2428.51	
Y36	VCCG0		1nv		-1088.1	-2428.51	
Y38	VSS	- Concert			-1583.4	-2428.51	
Y40		-defin.					
Y41	VCC	un		, de	-2574	-2428.51	
Y43	VCCGT	fer,		dui	-3069.3	-2428.51	ndefin
Y44	VCCGT	_		sine	-3564.6	-2428.51	
Y46	VCCGT			0°	-4059.9	-2428.51	Yeth
Y47	VCCGT		ed u		-4555.2	-2428.51	
Y49	VCCGT		Jefine -		-5050.5	-2428.51	
Y5	VSS		unos		8299.45	-2254.5	
Y50	VCCGT		0		-5545.8	-2428.51	
Y51	VCCGT	Aefil'			-6041.1	-2428.51	
Y54	VCCGT	unu		6	-6821.17	-2254.5	
Y56	VCCGT	ne ^o		dull	-7313.93	-2254.5	
Y58	VCCGT			sine	-7806.69	-2254.5 -2254.5 -2254.5	
Y60	VCCGT		_	der	-8299.45	-2254.5	194
Y62	VCCGT	ined undefin	-00	·	-8792.21	-2254.5	